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Ultrathin HfO_2(EOT < 0.75 nm) Gate Stack with TaN/HfN Electrodes Fabricated Using a High-Temperature Process

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High quality TaN/HfN/HfO_2 gate stacks with 0.65 nm of the equivalent oxide thickness and 0.3 A/cm^2 at (-1 V + V_{FB}) of the gate leakage have been demonstrated. An NH_3-based Si-surface nitridation process was performed prior to HfO_2 deposition. The HfO_2 films were deposited in a metallorganic chemical vapor deposition cluster tool. The TaN/HfN metal stacked layers were deposited on HfO_2 by reactive sputtering. The gate stack shows excellent thermal stability, in equivalent oxide thickness (EOT) and leakage after 1000°C annealing. A 10-year time dependent dielectric breakdown lifetime of 1000°C rapid thermal anneal annealed HfN/HfO_2 stack is projected at $V_g = -3$ V with an EOT = 0.75 nm.
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With the continuous scaling of the complementary metal oxide semiconductor (CMOS) technology, high-k gate dielectrics will be needed to replace conventional SiO_2 gate dielectrics for addressing the excessive high leakage concern.[1] HfO_2 has been considered as one of the most promising candidates for such applications.[2] Much effort has been made in developing a HfO_2 gate stack with equivalent oxide thickness (EOT) of less than 1 nm.[3-7] Although the as-deposited HfO_2-based gate dielectrics with metal gate electrode could achieve an EOT < 1 nm, a significant increase of both the EOT and the leakage current have been reported after the gate stack has been subjected to high temperature postmetallization annealing (PMA).[3-6] The increase of EOT during PMA has been speculated to be caused by either the reaction at the metal gate/HfO_2 interface and/or the poor oxygen diffusion barrier of the metal gate electrode. This thermal instability is a major concern for conventional gate-first CMOS processing. In this article, we have demonstrated a high-quality HfO_2 gate stack fabricated using NH_3-based surface nitridation prior to HfO_2 deposition in order to suppress interfacial oxidation at the HfO_2/Si interface as well as the HfN gate electrode that has been shown to be an excellent oxygen diffusion barrier.[8] Prevention of oxygen diffusion/penetration through the metal gate electrode during PMA is critical in controlling the final EOT. As a result, the EOT of the HfN/HfO_2 gate stack is successfully scaled down to 0.65 nm with excellent leakage of 0.3 A/cm^2 at V_{FB}-1 V. After 1000°C annealing, the EOT increases slightly to 0.75 nm with some reduction on leakage current and significant reduction on the hysteresis of the current-voltage curve (from 150 to 20 mV). These are the thinnest EOT and lowest leakage current values reported for high-temperature fabricated HfO_2 devices. We have also investigated time dependent dielectric breakdown (TDDB) characteristics of 1000°C annealed gate stack with an EOT = 0.75 nm.

MOS capacitors were fabricated on p-Si(100) wafers with 4-8 Ω cm resistivity. After HF-last pregate cleaning, the wafers were immediately loaded into a gate cluster system for HfO_2 deposition. The wafers received an in situ surface nitridation (SN) treatment in the surface preparation chamber in pure NH_3 at 700°C prior to HfO_2 deposition. After the SN, wafers were transferred under vacuum into the high-k deposition chamber. HfO_2 films were deposited at 400°C, followed by an in situ postdeposition anneal (PDA) at 700°C in N_2 for 1 min. A 50 nm HfN gate electrode with a 100 nm TaN capping layer was then deposited on HfO_2 by the reactive sputtering method.[8] After gate patterning by the reactive ion etching (RIE) process, postgate annealing (PGA) using rapid thermal anneal (RTA) in nitrogen ambient at 900-1000°C was performed for thermal stability evaluation. Finally, all devices received a forming gas (N_2:H_2 = 10:1) anneal (FGA) at 410°C for 30 min. The EOT is extracted using C-V simulation program taking the quantum mechanical effects into account.

Figure 1 shows the measured high-frequency C-V and I-V curves of TaN/HfN/HfO_2/Si gate stack with surface nitridation under different thermal treatments (FGA, 900 and 1000°C). Well-behaved C-V characteristics with excellent agreement with simulated C-V curves, as well as low gate leakage current densities are observed. The FGA sample shows an EOT of 0.65 nm with gate leakage of 0.3 A/cm^2 at V_{FB}-1 V. High-temperature PGA (1000°C) increases the EOT slightly by 0.1 nm along with some reduction of gate leakage, but reduces the C-V hysteresis significantly. This excellent thermal stability arises from the effects of both the surface nitridation and HfN gate electrode: the surface nitridation of Si substrates effectively suppresses the Si-oxygen reaction during HfO_2 deposition and the HfN gate electrode effectively blocks the oxygen diffusion during PGA. The measured C-V hysteresis values for the FGA, 900°C PGA, and 1000°C PGA samples are 150, 50, and 20 mV, respectively, indicating the PGA effectively reduces the bulk and interface traps of the HfO_2 gate stack, particularly when surface nitridation is used prior to high-k deposition.

Figure 2 plots the EOT and J_g at V_{FB}-1 V as a function of PGA conditions to elucidate the effects of surface nitridation treatment on the electrical stability of the ultrathin HfO_2 gate stack. As can be seen clearly, devices with surface nitridation treatment not only results in smaller EOT, it also reduces the leakage current effectively.

Figure 3 shows the cross-sectional high-resolution transmission electron microscopy (HRTEM) images of the FGA and 1000°C PGA HfN/HfO_2 gate stacks with surface nitridation treatment. The thickness of the interfacial layer of the FGA sample is ~0.4-0.6 nm and HfO_2 layer is about 2.5 nm. After 1000°C PGA, the interfacial layer increases slightly to 0.7-0.8 nm. The interface layer growth of ~0.2 nm is probably caused by the extra oxygen and/or moisture in the chemical vapor deposition (CVD) HfO_2 films

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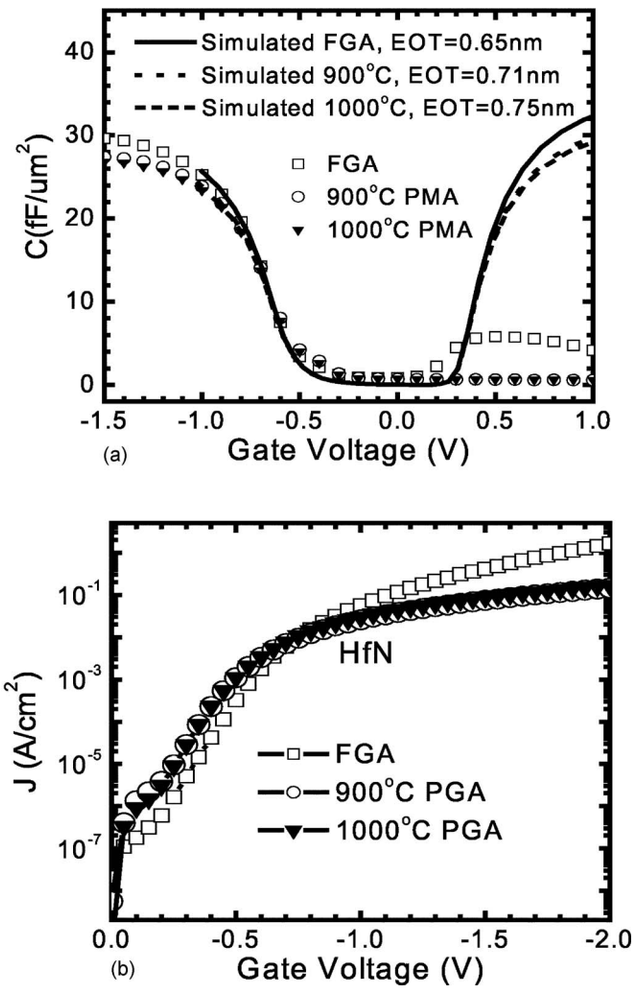

Figure 1. (a) High-frequency C-V and (b) *I-V* curves of TaN/HfN/HfO_2/Si devices after FGA, 900°C PGA, and 1000°C PGA with extracted EOT.

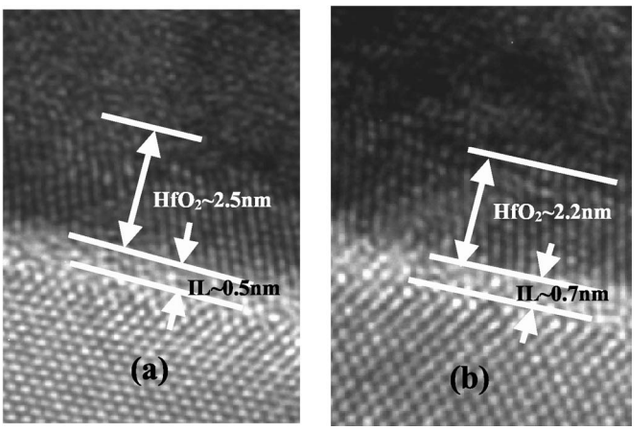

Figure 3. HRXTEM images of (a) FGA and (b) 1000°C PGA samples of HfN/HfO_2 gate stack with surface nitridation treatment.

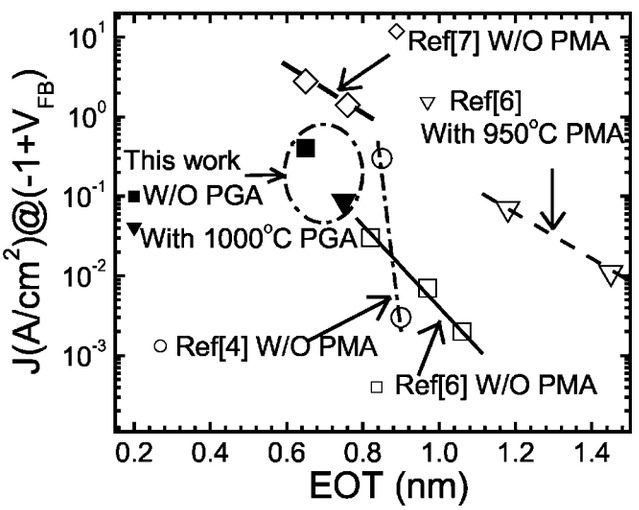

Figure 4. Comparison of the leakage current vs EOT for published HfO_2 gate stacks with EOT $<$ 1 nm including this work.

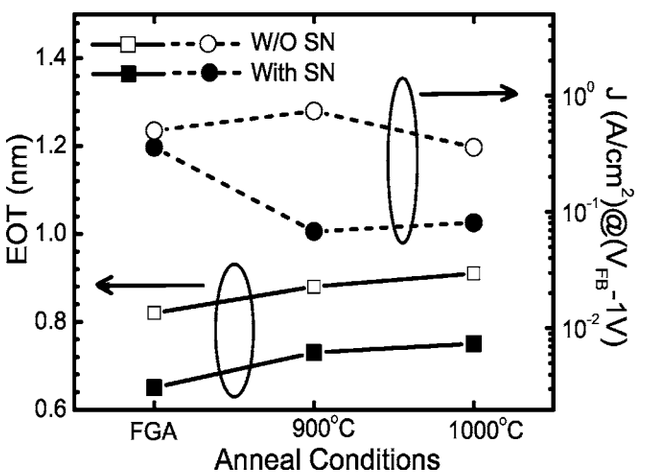

Figure 2. EOT and J_g at (-1 V + V_{FB}) as a function of PGA temperatures.

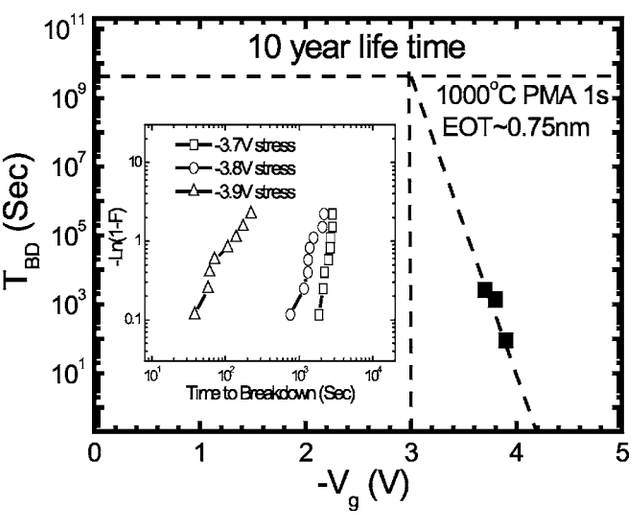

Figure 5. TDDB lifetime of 1000°C PGA HfN/HfO_2 gate stacks (EOT $\sim$ 0.75 nm) as a function of V_g at 25°C. A 10-year lifetime is projected at $V_g = -3$V.

that are released during PGA, resulting in oxidation of the HfO_2/Si interface layer. Compared to the FGA samples without SN,[9] the FGA sample with SN shows the thinner interfacial layer, which could be attributed to the antioxidation effect of the nitrided Si surface during HfO_2 deposition. Based on C-V and HRTEM results, the dielectric constant of the interfacial layer is estimated to be 7-9, very close to an oxynitride film. The increase of EOT mainly results from the increase of the interfacial layer.

Figure 4 compares the leakage current vs EOT of HfO_2 gate stacks from the data published most recently[4,6,7,10] including this work. The published data used physical vapor deposition, atomic layer deposition, or chemically vapor deposited HfO_2 together with TiN and TaN gate electrodes. A significant increase of EOT and leakage are observed in these devices after high-temperature RTA.

The TDDB characteristics of the 1000°C annealed devices with EOT = 0.75 nm were evaluated under constant voltage stress. A 10-year lifetime is projected at $V_g = -3$ V at 25°C, indicating excellent reliability (Fig. 5).

In summary, we have successfully demonstrated a high-k gate stack with very thin EOT, excellent leakage, superior thermal stability, and TDDB reliability using in situ processing including effective surface nitridation, CVD HfO_2, and PDA in a cluster tool, as well as a HfN gate electrode.

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