CLEANING TECHNOLOGY IN SEMICONDUCTOR DEVICE MANUFACTURING

Proceedings of the Seventh International Symposium

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PREFACE

The Seventh International Symposium on Cleaning Technology in Semiconductor Device Manufacturing was held during the Fall Meeting of the Electrochemical Society in San Francisco in September 2001. This series of symposia was initiated in 1989 during the Society Fall Meeting in Hollywood, Florida. Since then, the "ECS Cleaning Symposium" has become a bi-annual event of interest to all the members of the semiconductor community involved with advanced wafer cleaning technology. Reaching back we can identify several important new developments in silicon wafer cleaning science and engineering that were first introduced during the ECS Cleaning Symposia. Reflecting this trend the proceedings volumes from these symposia are consistently among the most popular proceedings published by the Electrochemical Society.

We hope the current edition will meet these high expectations in spite of the fact that the 2001 ECS Cleaning Symposium was not as well attended as symposia in this series in the past. The number of submitted papers was also lower. Both these facts are an obvious result of the slowdown the semiconductor industry was experiencing during 2000-2001. With drastic cuts in travel funds much fewer researchers and engineers from the industry were attending symposia and conferences. In those terms the 2001 ECS Cleaning Symposium was no exception. Fortunately, the scientific and technical quality of the papers presented during the symposium turned out to be immune to this overall negative trend.

We are very pleased that all papers presented during the symposium in San Francisco are included in this volume. They cover a broad range of topics of importance in state-of-the-art wafer cleaning technology and are divided into sections reflecting the distribution of emphasis in the contributed papers.

We would like to take this opportunity to thank all symposium authors and participants who turned this into a very informative and productive meeting. In particular, we would like to thank those among the authors who were involved in the preparation of the final camera-ready version of the respective manuscripts. Their responsiveness and willingness to cooperate with the editors is the main reason for which this volume appears in a timely fashion and in a shape hopefully meeting expectations of both readers and contributors. Our thanks are also due to the invited speakers for their excellent contributions and to all the participants for their encouragement and support. We are looking forward to the next symposium in this series in the Fall of 2003.

Jerzy Ruzyllo
Takeshi Hattori
Robert Opila
Richard E. Novak

TABLE OF CONTENTS

FACTS ABOUT THE ELECTROCHEMICAL SOCIETY

The Electrochemical Society is an international, nonprofit, scientific, educational organization founded for the advancement of the theory and practice of electrochemistry, electrothermics, electronics, and allied subjects. The Society was founded in Philadelphia in 1902 and incorporated in 1930. There are currently over 7,000 scientists and engineers from more than 70 countries who hold individual membership; the Society is also supported by more than 100 corporations through Contributing Memberships.

The technical activities of the Society are carried on by Divisions and Groups. Sections of the Society have been organized in a number of cities and regions. Major international meetings of the Society are held in the spring and fall of each year. At these meetings, the Divisions and Groups hold general sessions and sponsor symposia on specialized subjects.

The Society has an active publications program that includes the following:

Journal of The Electrochemical Society — The *Journal* is a monthly publication containing technical papers covering basic research and technology of interest in the areas of concern to the Society. Papers submitted for publication are subjected to careful evaluation and review by authorities in the field before acceptance, and high standards are maintained for the technical content of the *Journal*. Papers are published online as available at www.electrochem.org/publications/jes/journal.htm.

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Interface — *Interface* is a quarterly publication containing news, reviews, advertisements, and articles on technical matters of interest to Society Members in a lively, casual format. Also featured in each issue are special pages dedicated to serving the interests of the Society and allowing better communication among Divisions, Groups, and Sections.

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Proceedings Series — Papers presented in symposia at Society and topical meetings are published as serialized Proceedings Volumes. These provide up-to-date views of specialized topics and frequently offer comprehensive treatment of rapidly developing areas.

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For more information on these and other Society activities, visit the ECS website:

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ADVANCES IN WET CLEANING

SINGLE-WAFER SPIN CLEANING WITH REPETITIVE USE OF OZONATED WATER AND DILUTE HF ("SCROD")

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We have developed a new single-wafer spin cleaning technique that alternately cycles between ozonated water and dilute HF at room temperature and have implemented it in our advanced LSI production. During this cleaning, each solution is sequentially applied for only a few seconds onto a rotating silicon wafer using jet nozzles, and repeating the sequence to achieve the desired surface cleanliness. This process can efficiently remove particulate, metallic and organic contaminants from the silicon surface in a short time without any additives to the chemicals as well as without megasonic aids. This technique meets the requirements for stricter wafer cleanliness, larger diameter wafer processing, and greater respect for the environment. The mechanisms for the contaminant removal will be discussed with emphasis on the importance of the repetitive use of ozonated water and dilute HF.

INTRODUCTION

As semiconductor device geometries continue to shrink and die sizes grow, microcontaminants, such as particles, metallic impurities, and trace organic contaminants, will have an ever-increasing detrimental impact on device yield and reliability. Every wafer-processing step in ULSI manufacturing is a potential source of both particulate and metallic contaminants, which may lead to defect formation and device failure [1-3].

Scrupulous maintenance of the clean wafer surfaces throughout the wafer processing cycle is essential to obtain high yields during the manufacture of semiconductor devices [1-3]. Rigorous wet cleaning is known to be effective in reducing these contaminants from the wafer surfaces, making it the most frequently repeated step in any LSI manufacturing sequence [4-6].

Wafer-cleaning chemistry has remained essentially unchanged for more than 30 years [4, 5]. The most prevalent method worldwide is still hydrogen peroxide-based — most notably the RCA standard cleaning [7] — in which wafers are sequentially immersed for minutes in an NH_4OH-H_2O_2-H_2O mixture (or SC-1) and a HCl-H_2O_2-H_2O mixture (or SC-2) at elevated temperatures, as well as in dilute HF at room temperature. In some cases, a hot H_2SO_4-H_2O_2 mixture is added at the beginning of the sequence. In such immersion-type wet chemical cleanings, even if ultra-pure chemicals are introduced and then disposed of after each wafer cleaning treatment, the metal removal efficiency is

dominated by impurities brought into the fresh solution by the wafers to be cleaned [6, 8].

To meet the stricter wafer-cleanliness requirements, new cleaning methods, in which fresh chemicals are continuously supplied, such as single-wafer spin cleaning, have to be used. Single wafer processing equipment has the advantage of a much smaller footprint compared to a conventional wet bench, and is most suitable for short-cycle-time "minifab" operations for system LSI (or system-on-a-chip) production, to where the paradigm in semiconductor manufacturing has been being shifted from traditional high-throughput megafabs for dynamic RAM production. The throughput of the single-wafer processing equipment, however, must be increased and its chemical consumption reduced [9]. To solve this concern, the best approach is a technique using alternative cost-effective chemicals, rather than those conventionally used, and fewer chemicals to shorten the cleaning period and reduce chemical consumption. This also reduces the quantity of effluents from the wafer cleaning.

Not only particles and metallic contamination but also trace organic contamination, adsorbed on the surface of silicon wafers, is increasingly detrimental to semiconductor performance and yield. When silicon wafers are exposed to the atmosphere in a regular cleanroom, gaseous organic molecules in the air quickly adsorb on the wafer surface [10]. In addition, while wafers are stored in plastic boxes to protect them from airborne contaminants [10, 11], organic volatiles outgas from the plastic and are adsorbed onto the wafer surfaces [10-12]. Such organic contaminants have deleterious effects not only on the gate oxide integrity [13, 14], but also on the chemical vapor deposition [15]. It is as important to remove the organic contaminants as it is to remove particles and metallic contaminants from the silicon surfaces prior to subsequent processing [10].

In addition, as a trend in LSI device shrinkage, gate-insulator materials and their formation methodologies are to be changed from silicon dioxides thermally grown in a batch to silicon nitride/oxide gate stacks formed in a batch or with a single-wafer, and finally toward high-k dielectrics deposited by single-wafer atomic layer CVD. In accordance with this trend, pre-gate cleaning will naturally be changed from batch processing to single-wafer processing.

All these challenges are the reasons for the new single-wafer spin cleaning process we have developed. This process is low cost and environmentally friendly, has high performance at room temperature, and requires a short amount of time, alternating only ozonated DI water and dilute HF, for removing particles, metallics, and organics from the wafer surfaces [16, 17]. We call the process SCROD — single-wafer spin cleaning with repetitive use of ozonated water and dilute HF (Figure 1). In this paper, we will focus on the mechanisms of the particle, metal, and organic removals, with emphasis on the importance of the alternately cycling between ozonated water and dilute HF.

PARTICLE REMOVAL

To evaluate the SCROD process for particle removal, we used both Al_2O_3 and SiN particles as well as polystyrene-latex (PSL) spheres. The Al_2O_3 particles were chosen

because they are frequently found in wafer processing lines where equipment components are made from aluminum. Al_2O_3 particles are much more difficult to remove from a silicon surface than the PSL spheres and Si_3N_4 particles.

We used a standard sphere deposition system to deposit the PSL spheres onto 200mm diam. wafers. To deposit the Al_2O_3 or SiN particles on the wafers, we immersed the wafers in dilute HF, dipped them in deionized water in which the Al_2O_3 or SiN particles had been intentionally added, and then rinsed with DI water.

Following the preparation of the wafers, we subjected them to our SCROD single-wafer spin cleaning process, checking contamination levels and microroughness before and after cleaning. We detected the number of particles on the wafer to be ≥ 0.10 μm using an automated light-scattering inspection system.

SCROD applies ozonated water onto the center of a rotating wafer surface through a jet nozzle followed by the application of dilute HF through another nozzle. We varied the application time to determine the shortest time that provided acceptable results with a high reproducibility for volume production; this turned out to be 10 sec each for the ozonated water and dilute HF — a total of 20 sec for one cycle, but repeating this sequence as many times as needed. The concentrations of ozonated DI water and dilute HF were kept at 20ppm and 1%, respectively, throughout this study unless otherwise mentioned.

After the last dilute HF treatment, the wafer is rinsed with DI water and then spin dried in a nitrogen atmosphere to prevent water-mark (or drying spot) formation on the patterned wafer surface, as shown in Fig.2. All the cleaning and drying procedures were performed at room temperature (23°C). No additives to the chemicals, such as surfactants and chelating agents, as well as megasonic aids are needed for the SCROD cleaning.

We found that particles on the silicon wafer surface were very efficiently removed using this method. Figure 3 compares the particle removal efficiencies between the single-wafer spin SC-1 and SCROD. While one or three minute SC-1 spin cleaning can not remove the particles very well, the 1 min SCROD cleaning can remove the Al_2O_3, SiN and PSL particles very well —87%, 97%, and 99.5%, respectively. Thus, both the PSLs and SiN particles on the wafer surface were much more easily removed from the wafer surface than the Al_2O_3 particles. Even a one cycle repetition can remove the Al_2O_3, SiN, PSL particles by 79%, 86%, and 98%, respectively. The particle removal efficiency does not depend on the particle diameters down to 0.10 um, the minimum size we detected.

Let us now consider the mechanisms of particle removal. Figure 4 schematically summarizes the mechanism of particle removal. During the ozonated-water treatment, a chemical oxide film grows very rapidly on the wafer surface, becoming almost saturated at ~0.7nm after 10 sec of ozonated water application, as can be seen in Fig. 5. This chemical oxide can be completely etched from the wafer surface within 10 sec by the subsequent application of 1% HF and within 3 sec by 3% HF. The particle removal efficiency reaches its highest efficiency when the chemical oxide is completely "lifted-off" the wafer during the dilute HF treatment, as shown in Fig. 6. We have found that the particle removal efficiency depends on the etching depth of the chemical oxide, regardless of the HF concentration. The particle removal efficiency almost saturates

when a chemical oxide is completely etched from the silicon substrate. Therefore, applying the chemicals for a longer time (>10 sec each) does not increase the particle-removal efficiency [16, 17]. The particles removed from the wafer surface immediately flow away during spin cleaning so redeposition, which is often observed in the immersion-type wet chemical cleaning, is not observed even after the HF treatment. If some particles remain on the wafer surface, these particles are removed by the next cycles.

In addition to the silicon substrate, the SCROD single-wafer spin cleaning process can be successfully applied to thin films formed on the silicon surface, including silicon dioxide, silicon nitride, tungsten silicide, and polycrystalline silicon, by appropriately controlling the cleaning conditions such as the number of cleaning cycles and the dilute HF pouring time.

METAL REMOVAL

For the metal removal evaluation, Cu-, Fe- and Al- contaminated wafers were used. To prepare the Cu-contaminated wafers, test wafers were immersed in a dilute HF solution that was spiked with 10ppm Cu by adding a standard Cu-containing solution originally prepared for atomic adsorption spectroscopic analysis [17]. To prepare the Fe or Al-contaminated wafers, the test wafers were immersed in a contaminated SC-1 solution (NH_4OH-H_2O_2-H_2O) that was spiked with 1ppb Fe or Al by adding a standard Fe or Al containing solution. The contamination levels of Cu, Fe, and Al on the wafer surface were controlled within 10^{12} to 10^{14} atoms/cm^2 for each metal, and the metal contamination level and wafer surface were compared before and after the cleaning.

We measured the metallic contaminants on the wafers before and after spin cleaning using TXRF or flameless atomic absorption spectrometry (FL-AAS) after liquid phase decomposition of the contaminants. The detection limits for this technique are 1.5×10^8 atoms/cm^2 for Cu, 4.0×10^8 atoms/cm^2 for Fe, and 4.0×10^8 atoms/cm^2 for Al.

The Fe contaminants on a wafer surface as high as 10^{12} to 10^{13} atoms/cm^2 were reduced to the $\leq 10^9$ atoms/cm^2 with only one repetition of the 20-sec ozonated water and dilute HF treatment. Likewise, with just one repetition of the 20-sec treatment, the Al contamination was reduced to the 4.0×10^8 atoms/cm^2 detection limit.

The mechanism of metal removal is now discussed. Most of the Fe and Al atoms on the wafer surface were ionized and dissolved into the ozonated water. Some Fe and Al atoms remained in the chemical oxide grown during the ozonated water treatment because these atoms have a higher oxide generation enthalpy than silicon. However, the oxide-trapped atoms are dissolved when the chemical oxide on the wafer surface is removed with dilute HF. The Fe and Al ions dissolved in the dilute HF are not re-deposited on the wafer surface because these metals have a lower electronegativity than silicon. This accounts for the very high removal efficiencies of both Fe and Al.

The Cu contamination removal efficiency by only the initial ozonated water treatment as a function of ozonated water pouring time, is shown in Fig. 8(a). During the ozonated water treatment, the Cu contaminants are rapidly reduced on the wafer surface,

becoming almost saturated after 30 seconds of ozonated water application. Ozone has a higher oxidation-reduction potential than Cu, so ozone first oxidatively dissolves Cu, but the Cu contaminants are covered with a chemical oxide grown after a prolonged ozonated water pouring. The chemical oxide obstructs the dissolution of the Cu atoms by the ozonated water. Therefore, the Cu removal efficiency gradually decreases and finally saturates.

The Cu atoms remaining on the wafer surface after the ozonated water treatment are uncovered by etching of the chemical oxide during the subsequent dilute HF treatment. This treatment also removes Cu atoms incorporated into the chemical oxide by lifting off the chemical oxide. The uncovered Cu atoms are easily dissolved by the ozonated water treatment in the next cleaning cycle. Therefore, more ozonated water and dilute HF cleaning repetitions are effective in removing Cu compared to the longer chemical application time [16, 17]. Cu ions dissolved in the solution will not be redeposited onto the wafer surface because dissolved Cu ions immediately flow away from the wafer surface with spin cleaning. As the number of cleaning cycles increased, the surface contamination gradually decreased as seen in Fig. 7(b). Thus, Cu contamination is finally reduced to the 1 x 10^9 atoms/cm^2 level or lower using this repetitive cleaning method.

ORGANIC CONTAMINATION REMOVAL

To evaluate the organic-removal efficiency of the repetitive single-wafer spin cleaning using ozonated water and dilute HF, we prepared silicon wafers contaminated with butylhydroxytoluene (BHT) — one of the common antioxidants contained in plastic boxes. We also used silicon wafers stored in a plastic box for a long time in order to examine the ability to remove organic contaminants.

We analyzed the organic contaminants on the wafer using gas chromatography and mass spectrometry following thermodesorption (TD-GC/MS) [11], thus identifying the resultant molecular structures of the desorbed organic compounds by comparing the spectra from the mass spectrometer with library spectra data. To obtain a quantitative estimate of the residual organic molecules/cm^2 on the wafers, the peak areas for BHT in the resultant chromatograms were compared with those for standard samples of BHT whose concentrations were known.

We detected a large amount of 2,6-di-t-butyl-2, 5-cyclohexadiene-1, 4-dione (the oxidation product of BHT) and dibutyl phthalate (a plasicizer used in polymer molding) on the wafer stored in a plastic box before cleaning [11]. These organics were not detected after just one application of the ozonated water during the spin cleaning.

Intentionally contaminated BHT on wafer surfaces was reduced to $<10^9$ molecules/cm^2 (the detection limit of the TD-GC/MS) after one application of dilute HF following the ozonated water cleaning. Ozonated water has a sufficiently high oxidation potential to oxidatively degrade organic contaminants, while dilute HF is capable of removing them by lifting off the native oxide film on which the organic contaminants are adsorbed [11].

SURFACE ROUGHNESS

To evaluate the silicon surface roughness, we prepared highly doped surfaces by implanting and annealing As, producing a concentration of $\sim 10^{20}$ atoms/cm^3. Microroughness occurs more readily on an impurity-doped n^+-type surface [18]. We measured the microroughness on the silicon surface before and after the spin cleaning using an atomic force microscope (AFM).

The RMS measurements of the surface roughness before and after as many as 30 cycles of cleaning were 0.32nm and 0.33nm, respectively, thus virtually no difference. On the other hand, the simultaneous application of HF and ozonated water in a mixture causes a significant surface roughness, which is similar to the case of the SC-1 clean, a mixture of ammonia and hydrogen peroxide.

We concluded that repetitive SCROD spin cleaning did not produce a surface roughness compared to the simultaneous application of HF and ozonated water in a mixture that causes significant a surface roughness [19].

SEQUENCE MODIFICATION

When the initial native oxide film on wafers is >1 nm, due to prolonged exposure to ambient conditions, we recommend the application of dilute HF for more than 10 sec before applying any ozonated-water dilute-HF cycles. This will remove the thick native oxide and expose noble metals on the silicon surface and enhance the metal removal efficiency during subsequent cleaning. In our tests, Cu contaminants at $\sim 10^{14}$ atoms/cm^2 on a wafer with a relatively thick native oxide were removed to the 7×10^{13} atoms/cm^2 level by the ozonated water application. On the other hand, the same Cu contamination was reduced to 7×10^{11} atoms/cm^2 when we used dilute HF before the ozonated water application.

The final step of the SCROD cleaning process, after the last dilute HF treatment, includes two alternatives:

- A final DI water rinse renders a wafer with a hydrophobic silicon surface.
- A final ozonated water rinse renders a hydrophilic silicon surface.

GATE OXIDE INTEGRITY

Use of this cleaning technology, where fresh chemicals and water are continuously supplied, improves the gate oxide integrity of the MOS transistors compared to the conventional immersion-type RCA cleaning, where metallic contaminants accumulate in the solution. Figure 8 shows the time zero dielectric breakdown and time dependent dielectric breakdown (TDDB) of gate oxides prepared with the conventional-type RCA cleaning and SCROD cleaning. For both the TZDB and TDDB, SCROD gave better

results than the immersion-type RCA cleaning. This indicates that fresh chemicals and water are key factors in achieving a high gate-oxide integrity [8].

CHEMICAL AND WATER CONSUMPTIONS

SCROD markedly reduced the chemical and DI water consumptions compared to the traditional immersion-type RCA cleaning. As shown in Fig. 9(a), the liquid-chemical consumption for spin cleaning with three cycles of ozonated water and dilute HF is only 2.5 % of that used in the traditional RCA cleaning and 14 % of that used in an immersion-type dilute RCA in a single-bath system in which the chemicals must be renewed for each step.

In the standard immersion-type wet cleaning, the chemical solutions can be repetitively used to minimize chemical consumption, but metals accumulate in the solution, thus lowering the metal removal efficiency. Chemical solutions must be disposed of after each cleaning cycle to meet future metallic-contamination wafer-cleanliness requirements [8].

SCROD also reduces the volume of DI water required for wafer cleaning, which includes the water for rinsing the wafers and for diluting the chemicals and making ozonated water. If we assume that the water flow rate for wafer rinsing in the immersion-type systems is 25 liters/min, the DI water for spin cleaning with 3 cycle repetitions is 4% of the water required for the traditional immersion-type RCA cleaning and less than 2% for the spin cleaning with only one cycle (Fig. 9(b)). RCA cleaning, using both alkali and acid chemicals, needs a thorough DI water rinse for typically 10 min after each chemical treatment. Such rinsing is not necessary between the treatments of ozonated water and dilute HF in the spin cleaning.

EFFLUENT CONTROL

Hot liquid chemicals, such as NH_4OH, H_2O_2, and HCl, are used in the immersion-type RCA cleaning, so a large amount of highly concentrated gaseous chemicals are exhausted from large cleaning equipment. On the other hand, in a small spin-cleaning system that uses ozonated water and dilute HF at room temperature, the amount of exhaust is small and contains a low concentration of gaseous chemicals.

The effluents that do occur can be easily controlled in our spin-cleaning system.

- Disposed ozonated water spontaneously decomposes into oxygen and water.
- Disposed HF can be used to manufacture pure HF and other fluoride chemicals in the form of fluorite (CaF_2) in the chemical industry.

CONCLUSION

These are several driving forces toward single-wafer cleaning, such as more

stringent contamination control requirements, paradigm shifts in semiconductor manufacturing to shorter cycle-time minifabs for system LSIs, and changes in the gate-insulator materials and formation methodology.

We have developed a single-wafer spin cleaning at room temperature using only ozonated water and dilute HF without any additives to the chemicals as well as without megasonic aids. The spin-cleaning sequence consists of alternately applying ozonated water and dilute HF onto a wafer surface for typically 10 sec with 1% HF. This short-time cycle cleaning can efficiently remove particles and metallic contaminants as well as organic contamination without increasing the microroughness of the surface. This cleaning cycle can be repeated as many times as needed until the surface cleanliness reaches the required level. Furthermore, the 10-sec cycle can be shortened to a few seconds to save time, and chemical and water consumptions, if the concentrations of the ozonated water and dilute HF are increased.

In the final cleaning step, after the last dilute HF treatment, DI water is applied to the wafer to obtain a hydrophobic silicon surface or ozonated water to obtain a hydrophilic silicon surface.

This low-cost, high-performance, room-temperature treatment in which fresh liquids are continuously supplied will meet the requirements for stricter wafer cleanliness, larger-diameter wafer processing, and greater respect for the environment. We have already implemented this single-wafer cleaning procedure in our 200 mm and 300 mm fabs at Sony.

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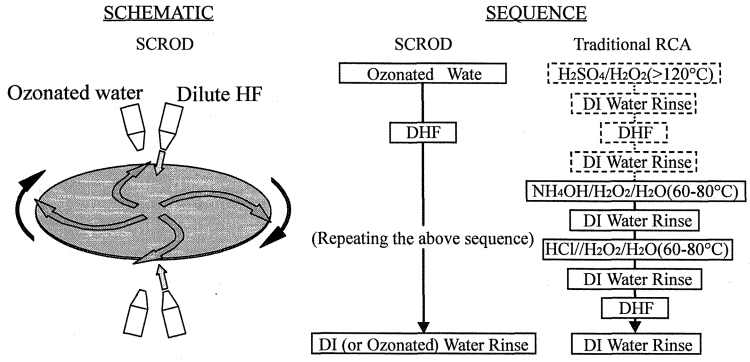

Figure 1. Schematic and sequence of the SCROD single wafer spin cleaning process.

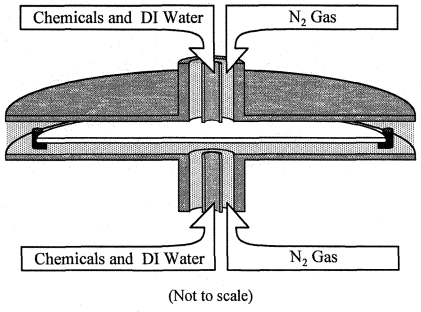

Figure 2. Schematic cross section of the single-wafer spin cleaning tool

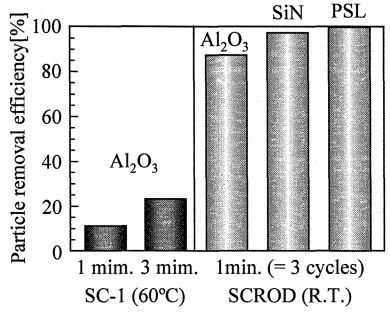

Figure 3. Comparison of the particle removal efficiencies between the single-wafer spin SC-1 cleaning and the SCROD.

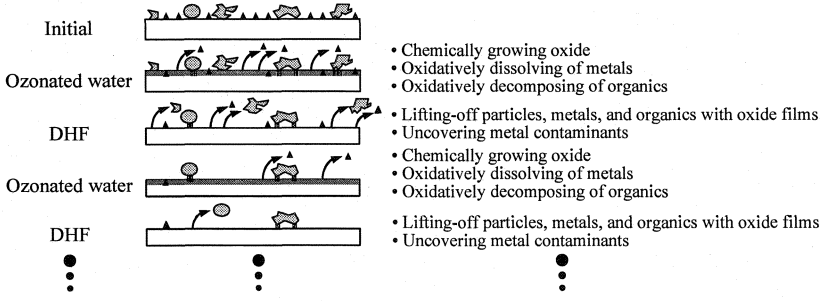

Figure 4. Schematic of the contaminant removal mechanisms.

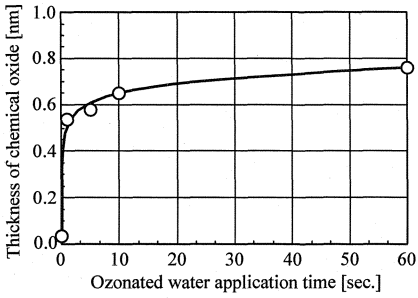

Figure 5. Thickness of chemical oxide on the silicon surface measured, using X-ray photoelectron spectrometry, as a function of ozonated-water application time.

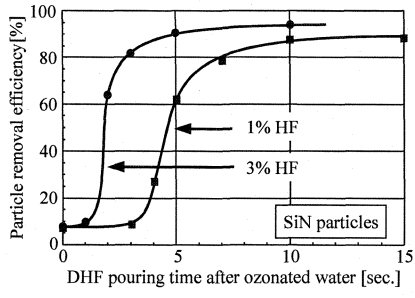

Figure 6. Particle removal efficiency after 1cycle cleaning as a function of dilute HF pouring time.

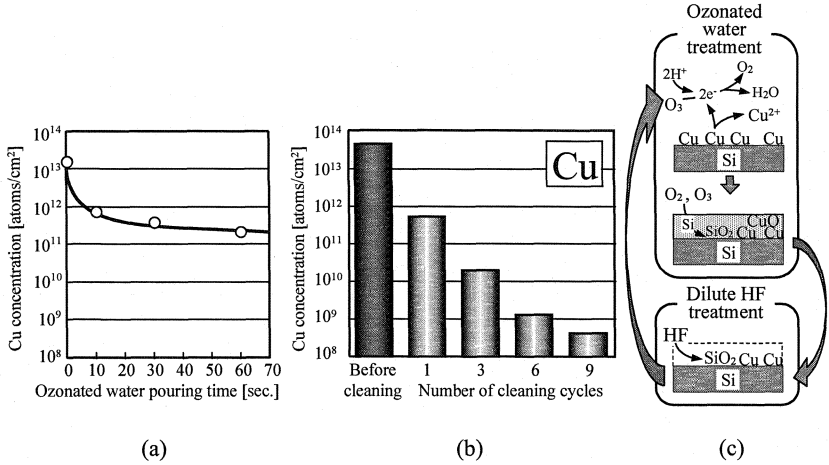

Figure 7. Cu concentration on a wafer surface before and after ozonated water pouring as a function of the application time (a). Cu concentration on the wafer surface before and after SCROD as a function of the number of cleaning cycles (b). Schematic representation of Cu removal from the silicon substrate (c).

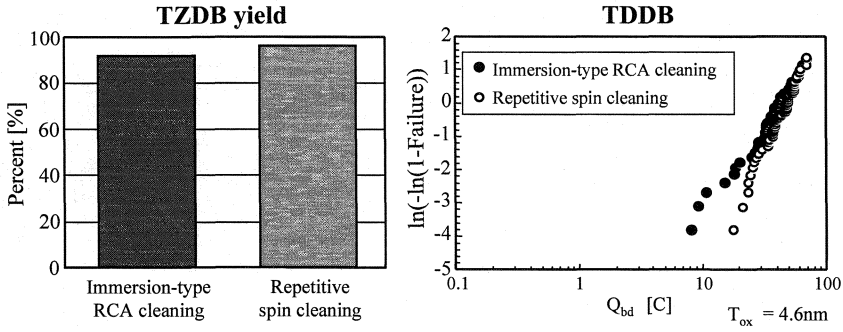

Figure 8. Comparison of gate oxide integrity for RCA immersion and SCROD repetitive spin cleaning.

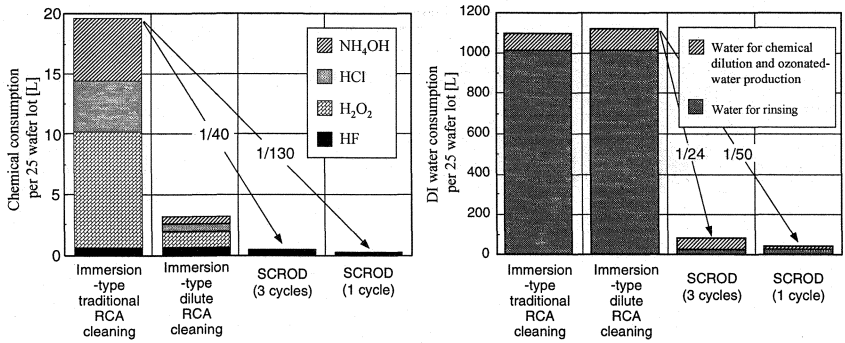

Figure 9. Liquid chemical (a) and DI water (b) consumption for a 25-wafer lot for the immersion-type RCA cleaning and SCROD spin cleaning. Assumptions include 3.5 x 10^4 cm^3 bath volume; traditional RCA cleaning steps of 10-min 1:1:5 SC-1, 10-min 1:1:6 SC-2, and 1-min 1% dilute HF; and dilute RCA cleaning steps of 10-min 1:1:50 SC-1, 10-min 1:1:60 SC-2, and 1-min 1% dilute HF.

EVALUATION OF NEW MEGASONIC SYSTEM FOR SINGLE WAFER CLEANING

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As for a megasonic single wafer cleaning system, we evaluated a "new" system in comparison with a conventional system. The main characteristics of this new system are that a quartz rod is set parallel to a rotating wafer and the megasonic wave is transmitted from the rod to the wafer through water. Although the new system has the same cleaning efficiency as the conventional system in the case of un-patterned wafer cleaning, it has a higher cleaning efficiency and lower damage than the conventional system in the case of high aspect ratio patterned wafer cleaning. We analyzed our data with the visualization of megasonic transmission using the Schlieren method and with the simulation using the Finite Difference Time Domain (FDTD). We found that in this new system, the megasonic wave propagates cylindrically from the quartz rod. Therefore, the wafer receives megasonic waves from perpendicular and various directions, resulting in higher cleaning efficiency. The gap between the quartz rod and the wafer to obtain this energy highest under limitation of mechanical accuracy is set at around 1 wavelength of megasonic wave in water. Furthermore, we found that lower damage of this system is caused by lower power density. However, the new kinds of damage caused by "edge effect" were observed. Therefore, to eliminate this damage will be the future issue of this new megasonic single wafer cleaning system.

INTRODUCTION

In recent years, we mainly use a scrubber type single wafer cleaning system for semiconductor manufacturing. This system has a high cleaning efficiency on flat or hydrophilic wafers. However, in the case of patterned or hydrophobic wafers, there is the possibility that "re-contamination" happened in this contact type system. This means that particles removing from a brush re-adhere onto a wafer. In a non-contact type single wafer cleaning system, for example, we use a megasonic and a water-jet system. As we used an immersion type megasonic cleaning system, we thought this system is "damage-free". When we moved toward a single-wafer type megasonic cleaning system, however, the damage happened at some conditions [1]. This phenomenon is explained with the cavitation, as seen in Fig. 1.

Fig. 1 shows the cavitation threshold curve [2]. The upper area of this curve is the cavitation zone and sometimes aluminum patterns of LSIs are damaged [1]. On the other hand, we had some information that a "new" megasonic system was designed at lower power density and had higher cleaning efficiency than a conventional megasonic system [3]. Fig. 2 shows schematics of the conventional megasonic system and the new megasonic system. As for the conventional megasonic system, a transducer vibrates vertically to a wafer and megasonic waves are propagated to a rotating wafer through water. On the contrary, in the new megasonic system, a quartz rod is set parellel to a wafer and a transducer vibrates horizontally. As a result of preliminary test, we found that this system makes no damage on aluminum patterns of LSIs. Therefore, we investigated the cleaning efficiency and damage in detail by this system. The results are also confirmed with the visualization of ultrasonic transmission using Sclieren method [4] and the simulation using Finite Difference Time Domain (FDTD) [5].

EVALUATION OF CLEANING EFFINCIENCY

We prepared the following two kinds of samples for the evaluation of cleaning efficiency: (1) Silicon nitride (Si3N4) films (without patterns) on silicon wafers, contaminated with polystyrene latex particles (PSL) with a diameter of 0.3 um. (2) Silicon dioxide (SiO2) films (with hole patterns) on silicon wafers, contaminated with PSL. There are three kinds of samples that the hole depth is 0.5 um, 1.0 um, and 1.5 um respectively with a diameter of 0.5 um. We measured the number of PSL on each sample using a particle inspection system, before cleaning and after cleaning with both the new megasonic system and the conventional one. The cleaning efficiency is defined as the particle removal ratio obtained through these measurements. The specifications of each system are shown in Fig. 2. The particle removal ratio for un-patterned wafers is shown in Fig. 3. We can see the new megasonic system has the same cleaning efficiency as the conventional one. On the other hand, for hole-patterned wafers, we found that the new

megasonic system has much higher particle removal ratio than the conventional one (Fig. 4). Obviously, in the conventional system, the particle removal ratio decreases drastically in proportion to the aspect ratio. On the contrary, in the new one, the particle removal ratio does not change even in a patterned wafer with a higher aspect ratio (e.g. aspect ratio is 3).

EVALUATION OF DAMAGE

We prepared samples of polysilicon (poly-Si) line patterns on silicon wafers for evaluation of the damage. Poly-Si patterns are seemed more sensitive to damage than aluminum patterns. There are four kinds of samples that the line height is 0.5 um, 1.0 um, 1.5 um, and 2.0 um respectively with a line width of 0.5 um. We measured the defect patterns of each sample using a defect inspection system, before cleaning and after cleaning with both the new megasonic system and the conventional one. The damage is defined as the defect density obtained through these measurements. The process specifications are the same as that of the evaluation of cleaning efficiency as previously described. The defect densities on poly-Si line patterned wafers are shown in Fig. 5. In the case of the conventional megasonic system, the defect density increases drastically in proportion to the aspect ratio. On the other hand, the defect density of the new one is very few. However, even for the new one, there are small defects distributed at the wafer edge and wafer center. We will discuss these phenomena later.

The results of cleaning efficiency and defect density indicate that the new megasonic system has a higher cleaning efficiency and lower damage on high aspect ratio patterns (Table 1).

VISUALIZATION USING SCHLIEREN METHOD

The visual observation of the megasonic transmission was achieved using the Schlieren method (Fig. 6) [4]. In this system, the deviation of refractive index caused by the megasonic wave in the water was optically observed with a charge coupled device (CCD) camera [6]. The Schlieren image in the case of only the quartz rod was set vertically in the water tank is shown in Fig. 7. The direction of megasonic wave is cylindrical from the quartz rod. It seems that the megasonic wave propagated parallel to the quartz rod, changed in the direction inside of the quartz rod. Furthermore, it also passes through from the quartz rod tip. Fig. 8 shows the Sclieren images when the quartz rod and a wafer were set vertically in the water tank. We changed the gap between the quartz rod and the wafer. When the gap is narrow, the strong wave is observed. The gap of this system is designed as around 1 wavelength, calculated by the megasonic frequency and the sound velocity in water.

SIMULATION USING FDTD METHOD

This simulation is to calculate the acoustic wave equation as how the megasonic wave propagates on the mesh divided quartz rod. The results of the simulation by FDTD [5] are as follows: (1) Megasonic waves are propagated in cylindrical direction from the quartz rod, as confirmed by the Schlieren image shown in Fig. 7. (2) The power density is calculated to be about 4 to 20 W/cm2. Concerning the former, we will explain in detail. Fig. 9 shows the mechanism of megasonic wave generation from the quartz rod. First, the incident waves from the transducer are propagated parallel to the quartz rod (Step 1). Next, the incident waves reflect at the quartz rod tip. The standing waves occur when this reflection waves interfere with the incident waves (Step 2). At the loops of the standing waves, the quartz rod is deformed toward cylindrical direction. When the quartz rod contacts to water, megasonic waves are propagated into water toward perpendicular direction from the deformed points (Step 3).

DISCUSSION

As we mentioned before, the megasonic waves are propagated into water in cylindrical direction from the quartz rod. Therefore, the wafer are received them from various directions. Furthermore, the gap between the quartz rod and the wafer is set at 1.8 mm where the megasonic energy is strong. The combination of these two factors allows a higher cleaning efficiency for the new megasonic system (Fig.10). As for the damage, the power density being calculated about 4 to 20 W/cm2 is located inside of no cavitation zone in the cavitaion threshold curve (Fig. 11). This implies low damage. However, we found that more sensitive patterns on the damage, like poly-Si patterns on high aspect ratio are broken even in this new megasonic system. It appears that the damage at wafer edge is caused by the local high power density at the boundary between water and air, and wafer center damage is caused by the strong megasonic waves passed through from the quartz rod tip (Fig. 12).

CONCLUSION

We found that the new megasonic system has a higher cleaning efficiency than the conventional megasonic system for high aspect ratio patterns and has also lower damage for fragile patterns, such as poly-Si patterns. Therefore, we will call this system "Soft Megasonic" system. However, the new kinds of damage caused by "edge effect" were observed. The new megasonic system should be controlled the power density both at the tip and at the other end of the quartz rod. To eliminate these damages will be the future issue of this new megasonic single wafer cleaning system.

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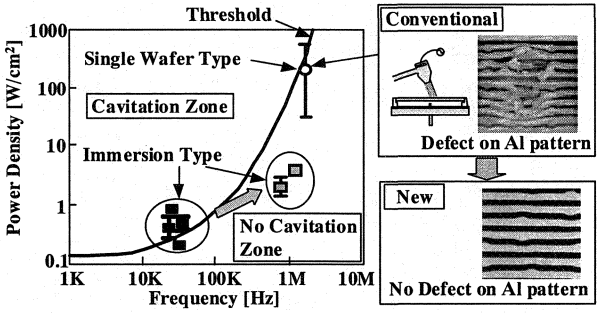
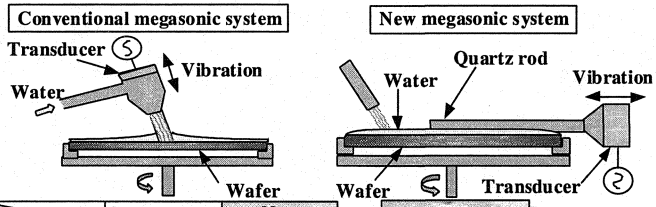


Fig. 1 Cavitation Threshold Curve



	Conventional	New
Frequency	1.5 MHz	0.835 MHz
Power	48 W	125 W
Power density	380 W/cm²	4 W/cm²

Fig. 2 Comparison of two Kinds of Megasonic Systems

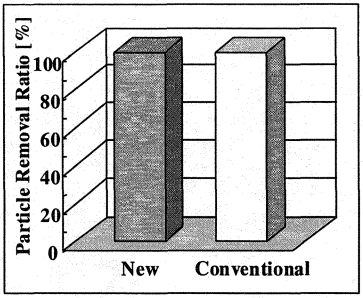


Fig. 3 Particle Removal Ratio on Si3N4

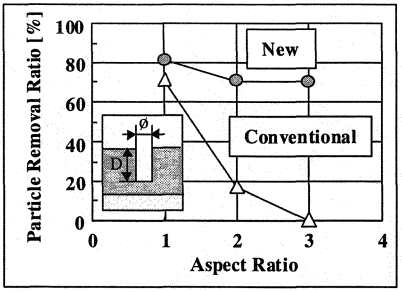


Fig. 4 Particle Removal Ratio in Hole Pattern

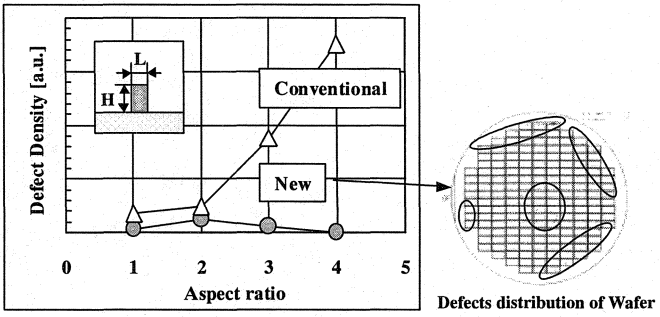


Fig. 5 Defect Density on Poly-Si Pattern

Table 1 Comparison of Cleaning Efficiencies and Damage

Evaluation item	Pattern	Film	Aspect ratio	Conven-tional	New
Cleaning Efficiency	Nothing	Si_3N_4	——	○	○
	Hole	SiO_2	1.0	○	○
			2.0	×	○
			3.0	×	○
Damage	Fine	Poly-Si	1.0	△	○
			2.0	△	△
			3.0	×	○
			4.0	×	○

○··· Good △··· Poor ×··· No Good

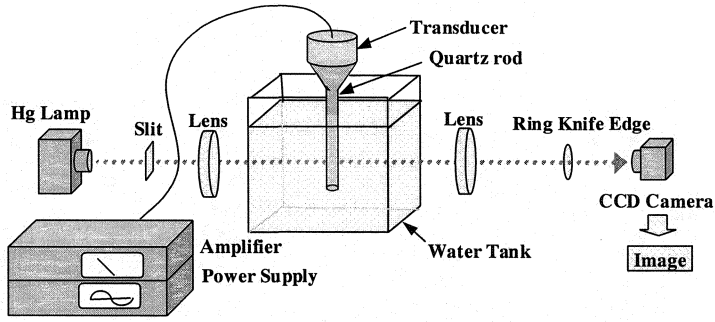


Fig. 6 Observation Setup of the Schlieren Method

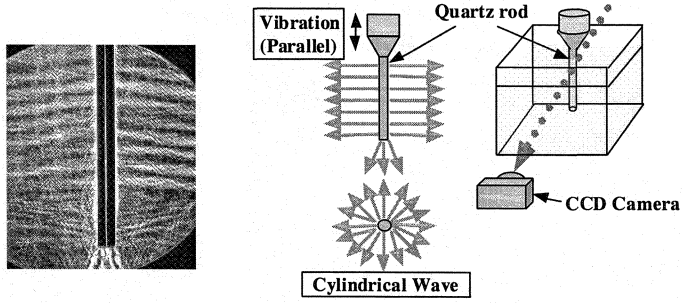


Fig. 7 Schlieren Image of Megasonic Propagation without a Silicon Wafer

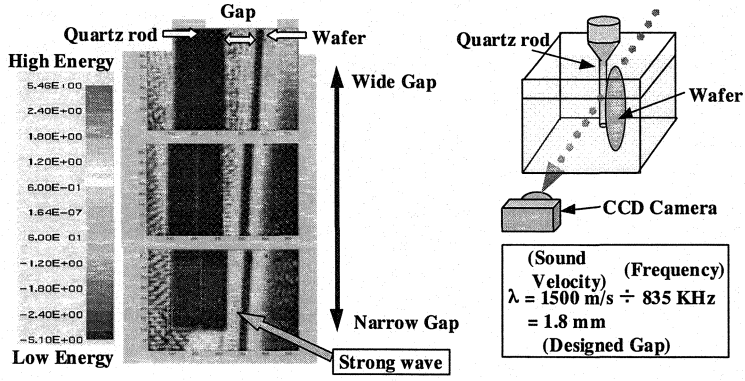


Fig. 8 Schlieren Image of Megasonic Energy Level with a Silicon Wafer

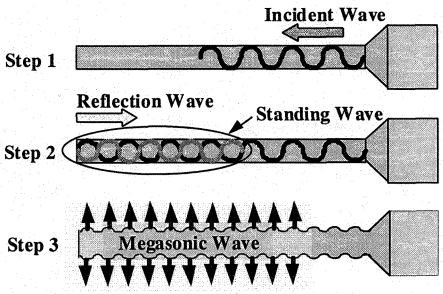


Fig. 9 Mechanism of Megasonic Wave Generation

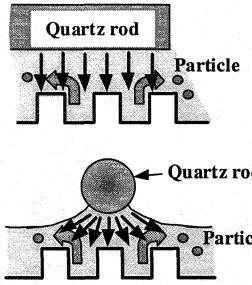


Fig. 10 High Cleaning Efficiency Model

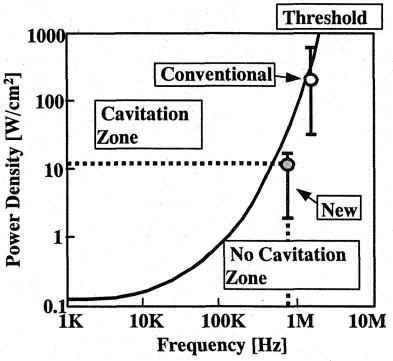
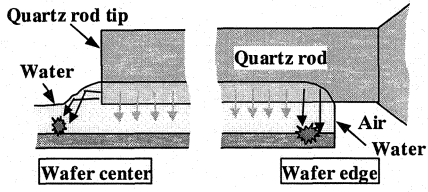


Fig. 11 Cavitation Threshold Curve



• Damage is caused by "Edge Effect"
(1)" Wafer Edge Damage " is caused by critical distribution of megasonic energy at the boundary between water and air.
(2)" Wafer Center Damage " is caused by megasonic energy passing through the quartz rod tip.

Fig. 12 Model of the Damage at Wafer Center and at Wafer Edge

ADVANCED SINGLE CHEMISTRY ALKALINE CLEANING IN A SINGLE TANK TOOL

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As dimensions scale down and government regulations are becoming stricter, the industry is moving to dilute single step cleaning, preferably with low etching and re-usable chemicals. In combination with a single tank tool this provides a high throughput process that can be run on a low footprint tool, economically translated: a low Cost of Ownership.
This article shows that APM+ -a chelating agent modified APM- run in a Single Tank Tool, is a good alternative for traditional cleaning sequences. APM+ is able to remove metals without risk for redeposition, without altering other APM properties like particle neutrality and removal. Electrical data show that a yield of almost 100 % is easily attained, compared to 0 % for the same chelating agent free APM solution with added metal contaminants, proving the possibilities of APM+ as an alternative for future cleaning.

INTRODUCTION

With regard to shrinking device size and ES&H demands becoming more and more stringent, the traditional RCA-clean (1, 2), has been subject of many changes. The cleaning roadmap is one of smaller footprints and diluted chemistries, e.g. replacing the SPM step by a SOM step or even an Ozone-DI-water step (3). While Single Tank Tools are conquering the market we are now moving on to Single Chemistry Cleaning. This reduction of steps combined with a reduction of the number of baths (STT) should lead to a high throughput process that can be run on a small footprint tool, meaning a further reduction in Cost of Ownership.
The conventional RCA-clean is an SC1 (APM or **A**mmonia **P**eroxide **M**ixture) step followed by an SC2 (HPM or **H**ydrochloric acid **P**eroxide **M**ixture) step. The first step is known to remove organic contamination and particles by continuously forming and dissolving a hydrous Si-oxide film. However a drawback of this solution is that it is prone to deposit metals on the wafer surface. This is due to the fact that some metals are insoluble in this caustic solution. The subsequent SC2 step is known to remove these residual metals. If the SC1 solution could be modified in such a way that metal deposition

is prevented, while maintaining good metal removal performance, it would ultimately enable us to omit the SC2 step. This leads to a Single Chemistry Clean with the above mentioned benefits.
Extensive research has already been done modifying the APM-step for single chemistry cleaning purposes (4, 5, 6, 7, 8). This report aims at proving some recent and most promising progress in this field, on a commercially available Single Tank Tool for 200mm wafers.

EXPERIMENTAL

The final metal concentration on the wafer surface after cleaning is determined by the equilibrium between precipitation of metals from the cleaning solution onto the wafer surface and removal of metals from the wafer surface. In order to study the impact of APM+ versus APM, we investigated these two processes separately by on the one hand processing clean wafers in a contaminated solution and on the other hand processing contaminated wafers with clean chemicals.
We used 200mm-wafers (Cz, <100>, p-type) and an imec-clean (O_3-HF-O_3) as preclean and reference blank. Metal contamination on the wafer surface was done using a spin-approach and yielded approximately 10^{12} at /cm^2 of Ca, Al, Zn, Cr, Ni, Fe and Cu. Alternatively the cleaning solution was in some cases contaminated with 1 w-ppb of the previous metals, which corresponds to a bath load after cleaning 50 wafers from 10^{12} to 10^{11} at/cm^2 in a 10 l bath. The cleaning solution was APM with volume ratio varying between 1/1/80 and 1/4/20 either as it is or modified by adding chelating agents (10-12 w-ppm, APM+). Subsequently the clean was followed by an acidic rinse (pH ~ 2) and Marangoni drying. All cleaning was done in a Mattson Single Tank Tool (STT200) installed in a clean room class 1. Surface metal concentration was evaluated by means of TXRF (**T**otal **X**-ray **R**eflection **F**luorescence) and AAS for Al (**A**tomic **A**bsorption **S**pectroscopy) (9).
The modification of the APM solution should have no harmful impacts on the other properties of this mixture. Therefore also particle neutrality and removal was checked. The latter was measured using SiO_2-particle contaminated wafers (>20000 LPD's/wafer, size > 0.12μmLSE) and a KLA-Tencor SP1-TBI. Finally APM+ was used as a pre-gate clean before capacitor fabrication (oxide thickness: 5 nm). Ramped voltage stress (E_{bd}, gate injection) was used for evaluating the gate oxide integrity (GOI). A breakdown field of 12 MV/cm was used as a yield criterion.

PROCESS EVALUATION

Metal deposition

In an APM metals tend to deposit metals onto the wafer surface due to the formation of less soluble metal hydroxides at high pH. However for some metals like Cu, Ni and Zn deposition is low because of relatively stable complex formation with ammonia (10). When moving to more dilute APM solutions, less ammonia is available for complex formation, resulting in an increased deposition of those metals. Figure 1 shows that in the

case of a contaminated 1/1/48 APM solution, bath loading or level of contamination in the bath, is more of an issue than in the case of 1/4/20 APM. An increase in deposition is observed for Cu, Fe and Zn. A contamination level of 1 w-ppb results in a re-deposition of ± 10^{12} at/cm² (Zn and Fe) when using 1/1/48 APM. The chelating agents should be strong enough to prevent not only the deposition in "concentrated" APM, but in addition to compensate for the loss of NH_3-based complexing potential in the case of diluted chemistries. Figure 1 shows that APM+ (1/1/48 +) significantly lowers the re-deposition compared to a 1/1/48 APM without complexing agents. Re-deposition is prevented to the same level when using 1/4/20 APM+ (no data shown). As temperature has already been shown to have an influence on the deposition behavior (8), temperature was varied. Generally increasing the temperature has almost no influence on the deposition behavior of non-modified APM. Figure 2 shows that also for the APM+ the influence of increasing the temperature is negligible compared to the impact APM+ has in general. The level of deposition remains unaffected for most metals except for Al, where there is a small further reduction in deposition observed. These data show that, from a metal deposition point of view, there is no real benefit working at higher temperatures. Figure 3 shows that

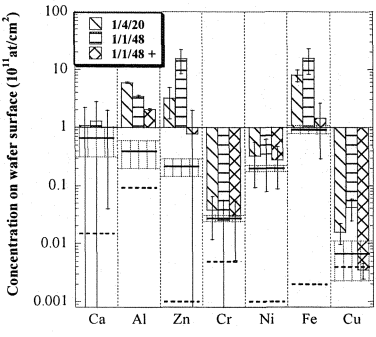

Figure 1: *Deposition of metals in different APM solutions at 35°C (dashed: detection limit, solid: blank)*

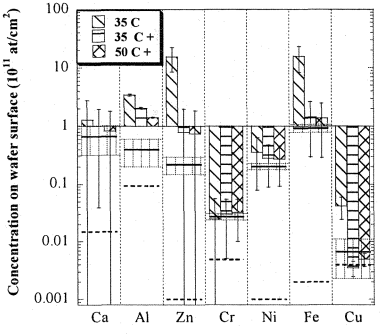

Figure 2: *Deposition of metals in 1/1/48 APM at different temperatures (dashed: detection limit, solid: blank)*

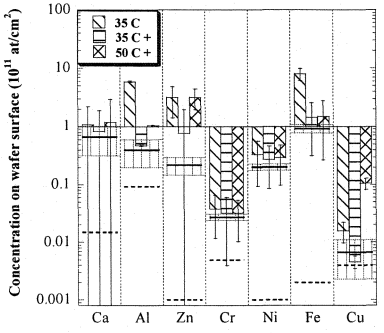

Figure 3: *Deposition of metals in 1/4/20 APM at different temperatures (dashed: detection limit, solid: blank)*

at a higher concentration of APM (1/4/20), deposition is prevented upon adding chelating agents to the solution. At this APM concentration however, an increase in temperature means also an increase in deposition. Likely the chelating agents are not stable enough to resist the relatively "aggressive" solution of 1/4/20 APM at 50 °C. Thus for the higher concentrations of APM, increasing the temperature is certainly no benefit with regard to deposition. The optimum in deposition prevention seems to be an APM solution of 1/1/48 at 35 °C.

Metal removal

In order for APM+ to have a future as a single chemistry clean, not only deposition of metals from the solution onto the wafer has to be prevented, but metal contamination must also be removed from the wafer surface. In a non-modified APM the equilibrium between both is more towards deposition, but with APM+ the metals, once removed, are kept in solution, which causes the equilibrium to shift more towards removal. Figure 4 shows that changing the concentration of the APM solution has no pronounced effect on the metal removal except for Zn, where the more concentrated APM shows better results. In general net removal is rather poor except for Ca. However if chelating

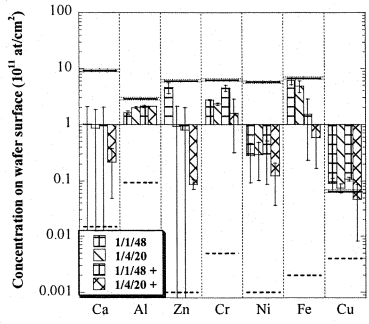

Figure 4: *Removal of metals in different APM solutions at 35 °C (dashed: detection limit, solid: reference 10^{12} at/cm^2)*

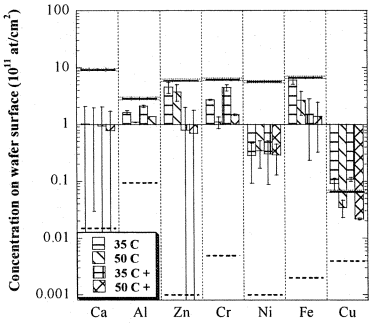

Figure 5: *Removal of metals in 1/1/48 APM at different temperatures (dashed: detection limit, solid: reference 10^{12} at/cm^2)*

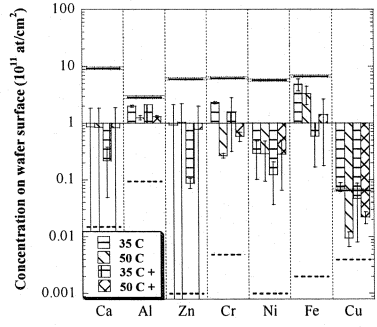

Figure 6: *Removal of metals in 1/4/20 APM at different temperatures (dashed: detection limit, solid: reference 10^{12} at/cm^2)*

agents are added to the solution, metal removal is improved and there is a clear APM-concentration effect observed. The combination of a higher APM concentration and adding chelating agents yields an increase in removal for almost all metals except for Al, and for Cu (only minor effect). Also here temperature was varied to check for effects on the kinetics of the reactions. Figure 5 and Figure 6 show that increasing the temperature for the non-modified APM is beneficial for all investigated metals except Ca, Zn and Ni. When chelating agents are added to a 1/1/48 solution, the same temperature dependence (see Figure 5) is observed and removal is improved. However an increase in temperature for the more concentrated APM (1/4/20 see Figure 6) is not bringing an additional benefit. On the contrary, the net removal of 1/4/20 APM+ at 50 °C is lower than at 35 °C. This confirms the observation for deposition where the assumption was made that the chelating agents are not stable enough in this more "aggressive" solution (see also Figure 3). As a rule of thumb, chelating agents improve metal removal independent of APM-concentration. However processing at elevated temperatures and concentrations adversely affects the performance and reduces the benefit of using APM+ over a standard APM.

Further dilution

Previous chapters have shown that APM+ works excellent, compared to APM, for low temperature and relatively high concentrated APM mixtures. Also for more diluted mixtures (1/1/48), APM+ shows a good performance. In this chapter we will evaluate whether this dilution can be further scaled. Figure 7 and Figure 8 show the deposition and removal behavior for 1/1/80 APM and APM+ solutions. In general for APM, the more

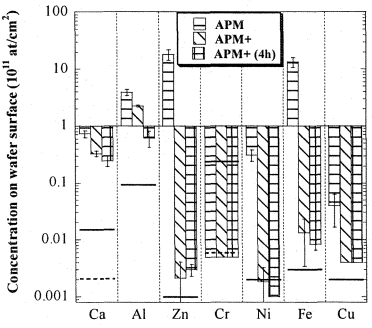

Figure 7: *Deposition of metals in 1/1/80 APM or APM+ (fresh or after 4h) at 35 °C (dashed: detection limit, solid: blank)*

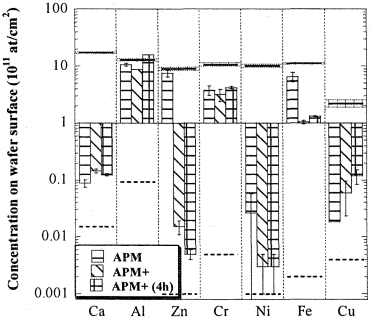

Figure 8: *Removal of metals in 1/1/80 APM or APM+ (fresh or after 4h) at 35 °C (dashed: detection limit, solid: blank)*

dilute, the more deposition of metals. As such the importance of adding chelating agents is prominent. Figure 7 shows that the APM+ is also for the 1/1/80 solution very effective in reducing the deposition below acceptable levels. More than 1 order of magnitude improvement for APM+ compared to APM for most metals. Even with a 4-hour-old

mixture the performance is unaffected, which proves the stability of the chelates for at least 4 hours (a typical bath lifetime). For Al a further reduction in surface contamination is observed after 4 hours, which indicates that the reaction of the chelating agent with Al is slow. Figure 8 shows that metal removal is improved when adding chelating agents to the solution. The removal of Zn, Ni and Fe is tremendously improved, Ca, Al and Cr respond more moderately to the modification. A 4-hour-old mixture shows the same removal behavior as a fresh mixture, which again confirms the stability of APM+.

PROCESS QUALIFICATION

Particle behavior

Modifying the APM solution to improve metal cleaning performance should not adversely affect the other properties. Therefore particle neutrality and removal efficiency was investigated for APM+ and compared to the non-modified APM.

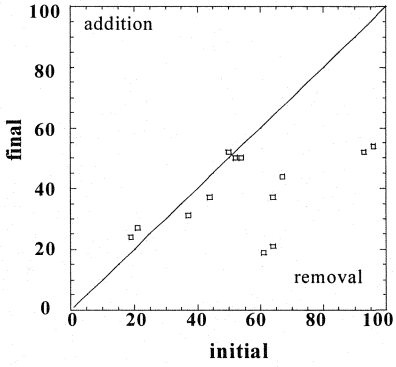

Figure 9: *Particle neutrality for 1/1/80 APM+ at 35 °C (ØLPD >0.12 µmLSE)*

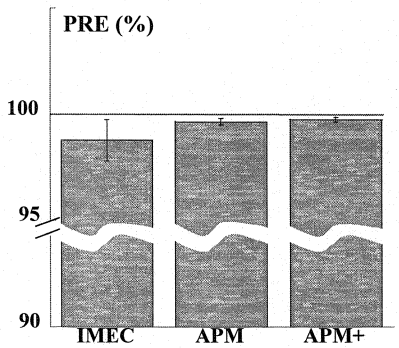

Figure 10: *Particle removal efficiency for different cleans (APM: 1/1/80 at 35 °C) initial SiO_2 particle count ~ 25000/wfr, measured at ØLPD >0.12 µmLSE*

Figure 9 shows the post-clean particle count (final) plotted versus the pre-clean particle count (initial). Everything above the 1:1-line indicates that particle addition occurred and under this line removal occurred. As only a few points are above the line, one can state that the APM+ process is at least particle neutral. Figure 10 shows the particle removal efficiency for the APM+ clean compared to the removal efficiency for a non-modified APM and for the imec-clean. It is obvious that the modification of the APM has no influence on the particle removal efficiency.

Electrical Qualification

The final test for every clean is the electrical qualification. We used an APM+ clean as a pre-gate clean in a capacitor lot. To enhance the effect of the chelating agents, cleaning was done with 1 w-ppb contaminated chemicals. As a reference condition capacitors were also grown on imec-cleaned wafers and on non-modified and non-contaminated APM and APM+ cleaned wafers.

yield		Acap (mm^2)		
(%)		9.7	2.8	0.9
Clean	imec	97.6	100	100
1/1/48	APM	98.8	98.8	100
	APM+	98.8	98.8	100
Cont.				
1/4/20	APM	0.0	0.0	0.0
	APM+	**98.8**	**98.8**	**100**
1/1/48	**APM+**	**98.8**	**100**	**100**
1/1/80	**APM+**	**97.6**	**100**	**98.8**

Table 1: *Yield for capacitors grown on wafers which received different pre-gate cleans (EBD, gate injection, yield criterion: 12 MV/cm, 84 capacitors per size)*

Table 1 shows that for non-intentional contaminated (i.e. clean chemicals) solutions, behavior is identical to the standardized imec-clean. This shows that the addition of chelating agents itself has no influence on the gate oxide integrity. It is only when bath loading (metal contamination) is present that chelating agents offer an advantage. Table 1 shows that when using contaminated chemicals (1 w-ppb) and a non-modified APM solution every device is defective. However if an APM+ is used a yield of almost 100 % is obtained, and this for every dilution investigated (even the ultra-dilute 1/1/80). This proves that the APM+ is a worthy alternative for standardly used pre-gate cleans and can hence be used as a single chemistry clean.

CONCLUSIONS

The purpose of adding chelating agents to an APM solution is to improve the metal behavior of the APM solution, allowing us to omit the HPM step, without altering the other properties of the solution.

In this paper we reported that metal deposition is prevented when adding complexing agents. Upon dilution APM loses part of its metal complexing properties. Adding chelating agents effectively recovers this property. A big improvement was observed for Fe and Zn, but also for the other metals (re-)deposition is below acceptable levels.

Metal dissolution is not improved for APM+ compared to APM, but metals, once removed from the wafer surface are kept in solution and prevented from re-deposition. The overall result is an improvement in cleaning efficiency or removal. Metal removal scales with increased APM concentration (e.g. 1/4/20). It is shown that the combination

of a 'higher' APM concentration and the use of chelating agents improves metal removal. Also in the case of very dilute APM (e.g. 1/1/80) a good metal removal was observed.
APM+ improves metal performance, while the clean remains particle neutral and the particle removal efficiency is unaffected. Particle removal efficiency was shown to be almost 100 %.
Ramped voltage stress tests have shown that adding chelating agents has no influence on oxide breakdown characteristics when clean chemicals are used. However if bath loading is present (metal contamination) a clear difference is observed. The APM clean yields only defective capacitors even at very low chemical contamination levels (1w-ppb). APM+ however shows a yield of almost 100 %, even when contaminated chemicals are used. The yield numbers show that even a 1/1/80 APM+ solution at 35 °C can effectively be used as a single chemistry pre-gate clean.
The feasibility of APM+ as a single chemistry alkaline cleaning method has been shown in a single tank tool. This yields a high throughput process that can be run on a low footprint tool. This new solution provides advantages on both the ES&H side and on the economical side. Cost reduction and 'green' cleaning go together well.

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NEW SHORT CYCLE WET CLEANING CONCEPT FOR A 300 mm FABRICATION LINE

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A new concept for short cycle time wet cleaning is investigated. It was found that using this concept, a typical 64 min HF-SC1-SC2 process can be reduced down to 2 min. The chemistry of this concept consists of a single step modified SC1 which replaces the dual step SC1-SC2. We have named this new cleaning concept, the AMAT clean.

INTRODUCTION

Shorter cycle times are necessary for a variety of reasons, such as rapid prototyping, smaller WIP and faster ramp of new technologies, tool qualifications and fab upstarts.
Wet cleaning is the most recurring process step in a VLSI manufacturing process. This process step suffers from very long cycle times. The example used is a traditional HF-SC1-SC2-dry cycle used in pre-thermal clean applications. This step currently has typically a 64 min cycle. This step by itself is usually repeated roughly 12-15 times in an entire VLSI process flow. The same applies to other similar wet cleaning steps such as SPM-SC1-SC2-dry. There are about 60-120 wet cleaning steps depending on the process flow.
In this paper, we will use the HF-SC1-SC2-dry cycle as a case study, but the results apply to most wet cleaning steps. We present here a new concept for short cycle wet cleaning that reduces the cycle time for this process down to 2 min, instead of 64 min. Surprisingly, even though the concept is a single wafer cleaning concept, the CoO of this new concept is similar or lower than the current conventional bathc wet bench HF-SC1-SC2 processing, which allows it to be used not only for rapid prototyping, but for volume manufacturing as well. Single wafer cleaning offers a variety of advantages in a production environment such as reduced cycle time & WIP, improved fab flexibility, reduced queue time management through matching of the throughput with other single wafer tools, reduced footprint and reduced water consumption. On top of that, there are a number of technical advantages to single wafer cleaning such as the elimination of the

cross contamination from the edge and the back of wafers, improved HF etching uniformity, reduced processing time and thus reduced side effects such as oxide loss, poly-Si loss, low-k absorption of liquids, improved contamination removal efficiency, improved interface control and last but not least integration potential with other tools.

AMAT CHEMICAL SINGLE WAFER CLEAN CONCEPT

The chemical concept of the AMAT clean is shown in fig. 1.

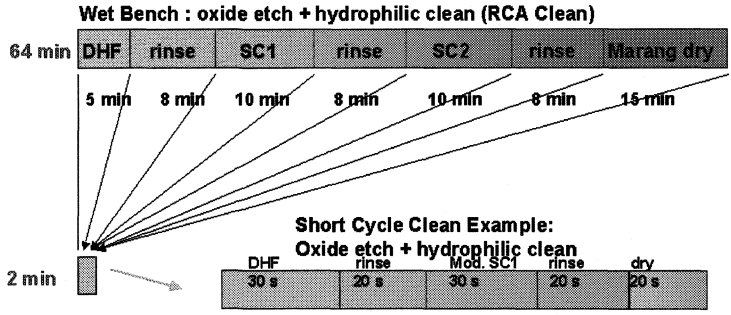


Fig. 1. Chemical concept to reduce the cycle time of HF-SC1-SC2 from 64 to 2 min.

The cycle time can be reduced as follows. The DHF etch can be reduced from 5 min to 30 s by using a horizontal spin and dispense/spray concept. Horizontal spin and dispense/spray allows very short etch times with very good uniformity. High concentration HF with very short exposure times can be used. The rinse can be reduced from 8 min to 20 s, by using the same concept and using centrifugal forces to reduce the boundary layer. In immersion wet benches, boundary layers of the order of 150 μm lead to rinse times of 8 min. In a horizontal spin system, the boundary layers are of the order of 10 μm, resulting in rinse times of the order of 20 s. The traditional SC1-SC2 cycle, where each step takes about 10 min, can be reduced into a single step of 30 s, by using the following concepts: the metal removal function of the SC2 can be combined into the SC1, by using a modified SC1, that includes chelating agents. The chelating agents take over the traditional metallic impurity removal function of the HCl, but work at high pH [1]. The SC1 itself can be reduced from 10 min down to 30 s, by using a much more efficient megasonics unit. Additionally, we have added surfactants to the SC1 to avoid any redeposition of particles and to achieve a total process time of 30 s. Finally, the drying relies mainly on the centrifugal forces to dry a wafer in 20 s.
This concept makes rapid prototyping possible.

PARTICLE REMOVAL EFFICIENCY

We evaluated the particle removal efficiency, using a modified SC1 for only 30 s with this single wafer system. We added chelating agents and surfactants to the SC1 to make 30 s processing successful.

We evaluated the Si_3N_4 particle removal at 0.12 μm and above both on the front side and the backside. We deposited Si_3N_4 particles in a random mode and in a spot. Starting Si_3N_4 particle counts were of the order of 2300 particles. A typical result on the

front side before and after a 30 s clean is shown in fig. 2 and 3 (front and backside) measured >0.12 μm.

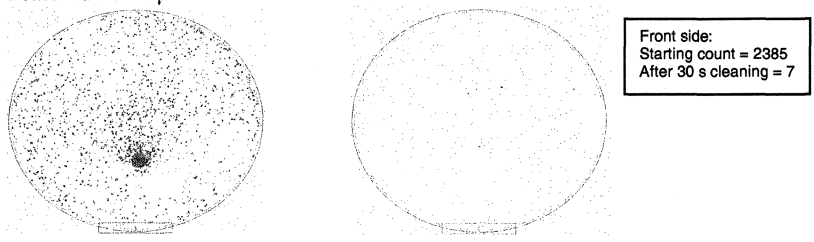


Fig. 2. Si_3N_4 particles before and after cleaning on the front side.

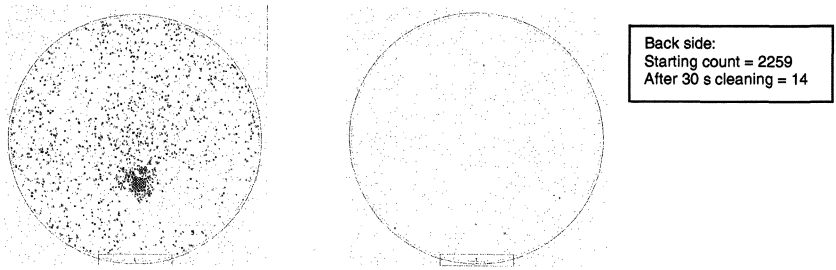
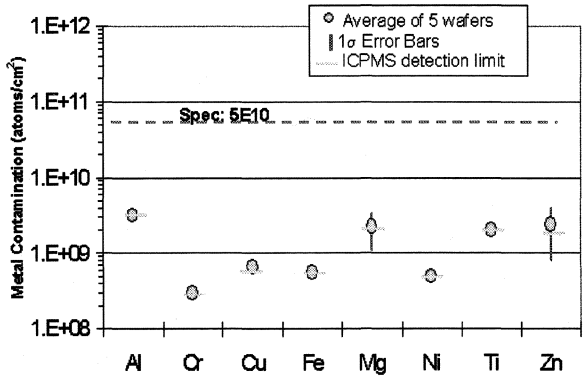


Fig. 3. Si_3N_4 particles before and after cleaning on the backside.

We also measured the thermal oxide loss. Due to the short process times, the thermal oxide loss is extremely small. In all cases, the thermal oxide loss for the modified SC1 in a single wafer mode is less than 0.1 nm.

METALLIC IMPURITIES

We measured the metallic impurities after this clean to validate the combination of SC1-SC2 into a single step. The metallic impurities after this clean are shown in fig. 4.



VPD-ICPMS Det. Limits (1E10 at/cm²)	
Al	0.3
Cr	0.03
Cu	0.05
Fe	0.05
Mg	0.1
Ni	0.05
K	0.3
Na	0.3
Ti	0.2
Zn	0.1

Fig. 4. Metallic impurities after the modified SC1 process

As can be seen from fig. 4, all common metallic impurities are below the VPD-ICPMS detection limit, which is of the order of 1e8 at/cm^2 to 1e9 at/cm^2.

ORGANIC RESIDUES

We have selected chelating agents and surfactants, which can be completely rinsed. First, we measured the characteristic peaks in a TOFSIMS spectrum of the chelating agent and the surfactant, by depositing a concentrated solution on the wafer and letting it dry to the air. This is shown in fig. 5. Then we looked for these peaks after the short cycle clean (modified SC1) followed with a rinse. No organic residues were found with TOFSIMS as shown in fig. 6.

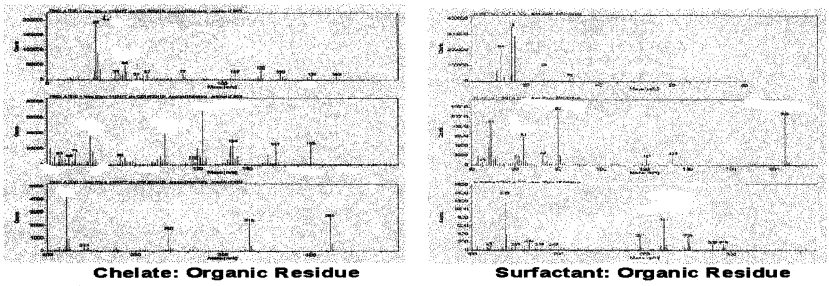


Fig. 5. TOFSIMS spectra from the chelate and the surfactant residue on the wafer.

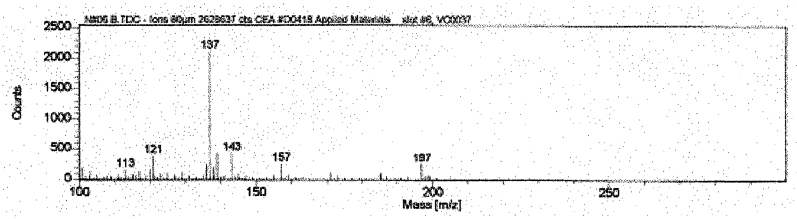


Fig. 6. TOFSIMS spectra after modified SC1+rinse.

SUMMARY

In this paper we have presented a new concept, called the AMAT clean and the feasibility data of this short cycle wet cleaning process that is equivalent or better than a conventional batch wet cleaning. We have shown that the particle removal efficiency is better or equivalent to a 10 min conventional wet bench process. At the same time, no damage to 0.1 μm poly-lines was observed and less than 0.1 nm of thermal oxide loss was measured. Metallic impurities are below the detection limits and no organic residues were found with TOFSIMS.

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ORGANICS

IMPACT OF CARBON CONTAMINATION ON DEVICE PERFORMANCE

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For 130 nm technologies, the 1999 ITRS Roadmap indicates that the level of organic contamination after critical cleans should not exceed 5.3E13 carbon atoms/cm^2. This paper explores the validity of this roadmap value through a quantitative evaluation of carbon impact on device performance. The evaluation utilizes a methodology for controlled carbon introduction into a gate dielectric film together with a SIMS measurement for quanifying organic levels; electrical characteristics of transistors are then compared. Results suggest that high carbon levels are detrimental, but that lower levels (1E13 atoms/cm^2) have minimal device impact. Data in this study support the values proposed in the ITRS Roadmap.

INTRODUCTION

Organic contamination of wafer surfaces remains a serious concern within the microelectronics industry due to the ability of organics to degrade gate oxide integrity. The 1999 ITRS Roadmap indicates that organic contamination after critical cleans should be below 5.3E13 carbon atoms/cm^2 for 130 nm technologies. Roadmap values, however, are based on interpretation of limited experimental data in the literature [1, 2].

Numerous researchers have explored the impact of organic contamination on devices [3-7]. These past studies concentrated on identifying organics on wafer surfaces, and have relied upon the techniques of time-of-flight secondary ion mass spectroscopy (TOF-SIMS) and thermal desorption – gas chomatograph – mass spectroscopy (TD-GCMS). These techniques, however, don't allow a quantitative assessment of carbon trapped at oxide-poly interfaces after gate stack formation. It is the amount of carbon incorporated into the dielectric which impacts device performance, and this does not always correlate well with the amount of carbon detected on bare surfaces prior to high temperature gate stack processing.

Guan, et al. [8] recently discussed the use of SIMS depth profiling to probe carbon contamination in oxide-polysilicon gate stacks. A SIMS methodology was utilized to explore the amount of carbon trapped within a gate stack after various pre-gate clean strategies, but carbon impact on device response was not addressed. In the current investigation, quantitative levels of entrained carbon are correlated with electrical performance of transistors.

EXPERIMENTAL

Wafer Preparation

This evaluation utilized unpatterned test wafers and NMOS transistor wafers. All processing occurred at International SEMATECH. Carbon was intentionally introduced to wafers by ion implantation through a 15 nm sacrificial oxide layer; the possible impact of implantation damage was not explored. Four different doses of carbon (0, 1E13, 1E14, 5E14 atoms/cm^2) were evaluated in the study; implantation energy was 10 keV in all cases. After the sacrificial oxide was stripped in the pre-gate clean, an oxynitride gate dielectric was grown. On unpatterned wafers used for SIMS profiling, the dielectric was 4.5 nm thick. NMOS transistors used in the evaluation were fabricated with gate dielectric thicknesses of either 2.5 nm or 4.5 nm. In all instances, oxidations were performed with an in-situ steam generation (ISSG) technique; the 2.5 nm films were grown at 950 C, while 4.5 nm films were grown at 1050 C. O_2 was set to 4.95 slpm, and H_2 was 50 sccm regardless of film thickness. All wafers were subjected to a post deposition anneal at 900 C with 2 slpm of NO.

SIMS Profiling

Profiles of carbon in 4.5 nm oxynitride films were obtained using dynamic SIMS depth profiling. For the analysis, a Physical Electronics ADEPT-1010 was utilized. Carbon (C) was monitored as a negative ion under Cs^+ bombardment at an impact energy of 10 keV and a 60° angle of incidence. Secondary ions were collected from the center 2% of a 400 μm x 400 μm rastered area. A 1 cm^2 piece was taken from the center of each wafer, and three profiles were acquired from each piece. Atomic concentrations of C were determined using a relative sensitivity factor (RSF) for C in Si calculated from an implanted standard. The raw data was normalized to the ^{30}Si signal before doses were measured. Stylus profilometry was used to determine the depth scale for the profiles.

RESULTS AND DISCUSSION

Carbon Profiles

Figure 1 shows a SIMS depth profile for a sample implanted with 5E14 atoms/cm^2 of carbon. No carbon is detected in the the polysilicon cap (top 200 nm). There is a clear

concentration of carbon in the oxynitride film, but the image also indicates that some C may remain in the silicon under the oxynitride film with this contamination methodology. Table 1 provides a summary of the carbon dose detected by SIMS for each implantation dose; values are obtained by averaging the results for all wafers at that dose. The SIMS technique did not find any carbon in the oxide of samples which were not implanted, and a detection limit of 1E12 carbon atoms/cm^2 has been estimated. Precision improves at higher implantation doses due to the diminishing impact of the background signal. Note that some of the C implant would have been retained by the sacrificial oxide and then lost during oxide removal; it's also speculated that the calibration standard used (C implanted into Si) may not be completely accurate for a sample that is largely C contained within oxide.

Transistor Electrical Performance

Transistor parameters were measured on devices with a 10 μm gate width at gate lengths varying between 0.15 μm and 1.00 μm. Threshold voltage (V_t) values for various channel lengths are presented in Figure 2; each symbol represents an average of values obtained from three wafers at the given dielectric thickness and carbon dosage. Error bars represent +/- one standard deviation. V_t is seen to decrease with increasing carbon dosage, with a dramatic drop as C dose moves from 1E14 to 5E14. The C-V data (below) helps clarify that for low carbon levels, the primary mechanism for V_t variation is a carbon-induced film thickness variation. At the highest C doses, Vt is also influenced by positive charge build-up.

Figure 3 shows transconductance for 0.25 μm channel length devices. While a difference between G_m in 2.5 nm dielectrics and 4.5 nm dielectrics is noted, a strong impact from carbon is not apparent with the 4.5 nm dielectrics. High carbon doses have greater effect on G_m for the thinner dielectric devices since positive charges associated with carbon ions are effectively closer to the dielectric/silicon interface.

Breakdown voltages (V_{bd}) were measured for 4.5 nm and 2.5 nm oxide films using positive bias (inversion) voltage sweep in 0.1 V step increments. Breakdown was considered to have occurred when a current of 1 μA was reached. Figure 4 shows the distribution of breakdown voltages found on the tested wafers; three wafers of each dielectric thickness/carbon dosage combination were measured. Figure 4 indicates that the wafers with the largest carbon doses had the lowest breakdown voltages.

Gate leakage current was measured in inversion at V_g = 1.8 V. Results of gate leakage measurements are shown in Figure 5. Figure 5 suggests that the introduction of carbon may increase gate leakage current, but it is possible that this effect is driven mostly by the influence of carbon on electrical oxide thickness (see below).

Electrical oxide thicknesses were calculated from C-V data using a quantum effects correction methodology [9]. Results suggest that the presence of carbon in silicon

significantly suppresses oxide growth. Figure 6 shows results of electrical oxide thickness (EOT) measurements for all carbon doses; Figure 7 focuses in on the 2.5 nm devices to give greater resolution to the data. For both dielectric thicknesses, the data shows reduced EOT with increased carbon content. Physical measurements of the oxide thickness were not made.

Figure 8 is a C-V curve for 10^{-4} cm^2 capacitors with 2.5 nm dielectric films. The shift in the curve at a dosage of 5E14 indicates a build up of positive charge in the oxide. Recall (Figure 2) that a significant V_t shift at doses beyond 1E14 is consistent with a carbon-related charge build-up. Another feature of note in the C-V curve is the 'kink' towards the bottom of the curve for high doses. This suggests the existence of interface states. This observation is in agreement with the transconductance observation; G_m will be sensitive to interface states, and Figure 3 indicated a reduced G_m for high carbon doses on 2.5 nm devices. Evidence of interface state generation appears stronger with 2.5 nm dielectrics than with 4.5 nm dielectrics (Figure 9) in this study.

Transistor Reliability

Reliability testing involved constant voltage Qbd and Stress Induced Leakage Current (SILC) measurements. During SILC testing, a sense voltage of 1.5 V was applied; the stress voltage in the test was 4.7 V for 2.5 nm dielectrics and 6.9 V for 4.5 nm dielectrics. Data indicate that leakage current increases as the amount of carbon increases. Figures 10 and 11 illustrate the yield trends from SILC testing; the graphs show the % of passing die that exist after each sequentially longer stress event. For this evaluation, a SILC failure is considered to have occurred if the current increases more than 10X after a stress event. These data indicate that 4.5 nm devices are more sensitive to carbon implantation than 2.5 nm devices due to greater film thickness reduction. Time to dielectric breakdown was also considered in this study. A 'breakdown' in this case occurs when the current measured during a stress event (J_{stress}) increases more than 10X over the previous measurement. As with SILC failures, carbon is found to degrade reliability.

Finally, charge to breakdown was considered for each combination of oxide thickness and carbon dose. Figure 12 summarizes the average charge to breakdown for each condition. This plot shows the charge at which a hard failure occurs and the charge at which a 'first' failure (hard or soft) occurs. A hard breakdown is said to occur when the stress current increases more than 10X over two consecutive measurements; a soft breakdown is reported when the variance for a group of five consecutive data points increases by more than 100X. Figure 12 demonstrates that carbon is detrimental for device reliability even at a dose of 1E13.

CONCLUSIONS

This evaluation indicates that carbon contamination can significantly degrade gate oxide quality and gate oxide reliability. While the primary effect from small doses of

carbon is suppression of electrical oxide thickness, higher doses of carbon show the generation of interface states and positively charged centers in bulk oxide.

With the oxide growth process used in this study, the quality of thinner oxides appears to be more sensitive to substrate carbon contamination than the quality of thick oxides. Interface state generation was an issue for 2.5 nm dielectrics but less for 4.5 nm dielectrics. In part this could be caused by the use of different oxidation temperatures for the two dielectric thicknesses.

Overall, this study indicates that high carbon content (dose of 5E14) is detrimental while doses closer to 1E13 have minimal impact. While some parameters (EOT and charge-to-breakdown) showed carbon impact at low doses, the impact doesn't become dramatic until doses exceed 1E14. These data would therefore indicate that the values proposed in the 1999 ITRS Roadmap for allowable organic contamination are reasonable. Even if all of the carbon on a wafer surface after pre-gate clean becomes trapped within a dielectric layer (a worst-case scenario), E13 levels of contamination on a wafer may be tolerable.

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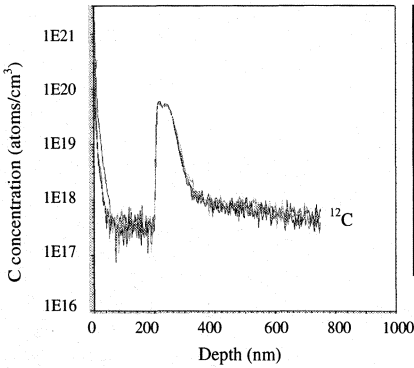

Figure 1: SIMS depth profile of C^{12} in a sample with a 5E14 implantation dose

Table 1: Average implanted dose vs. SIMS-measured dose in gate stack

Implant Dose	Average Measured SIMS Dose	std dev
0	0	-
1.00E+13	3.96E+12	3.68E+11
1.00E+14	4.35E+13	2.63E+12
5.00E+14	3.04E+14	7.73E+12

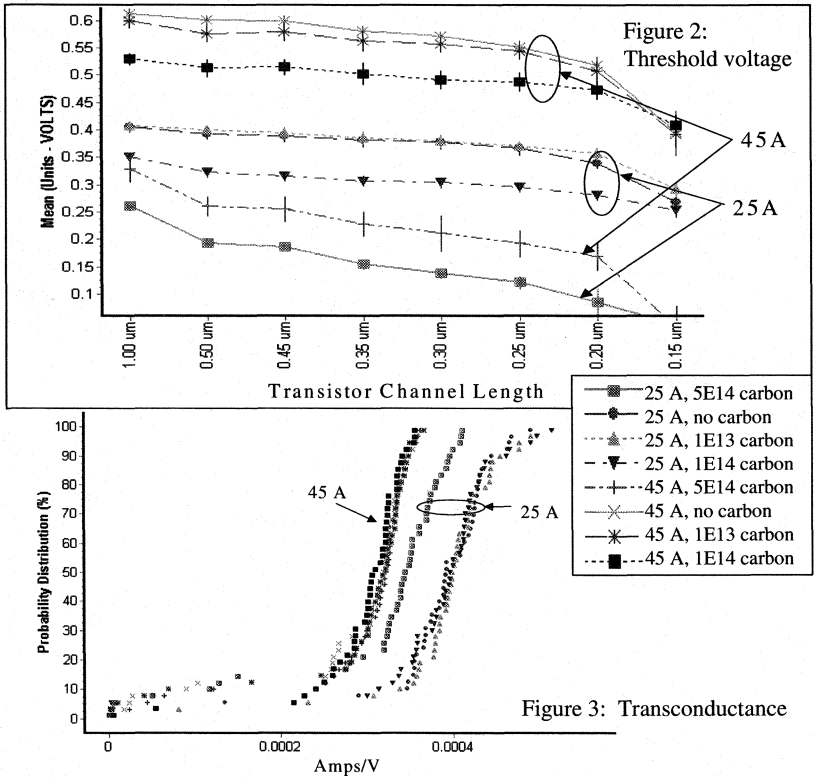

Figure 3: Transconductance

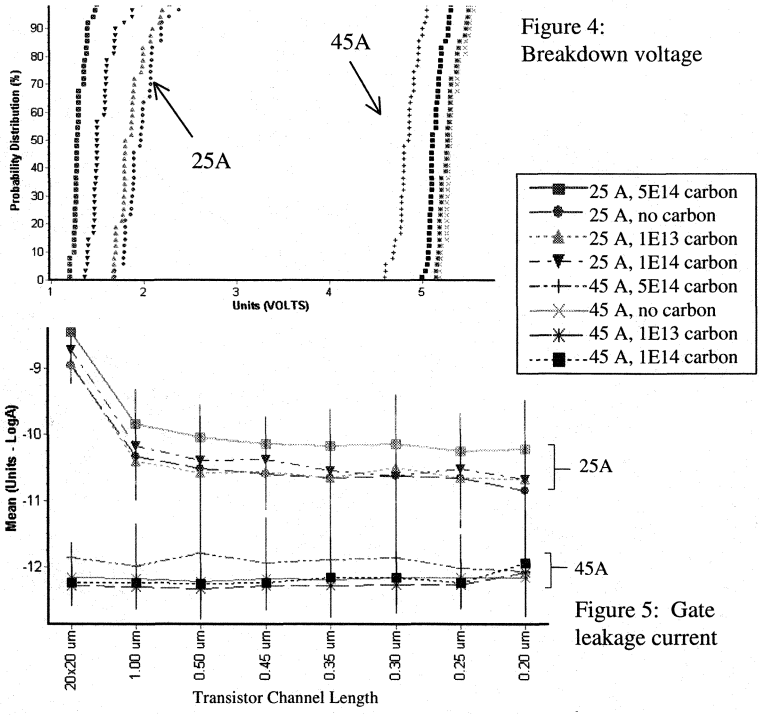

Figure 4: Breakdown voltage

Figure 5: Gate leakage current

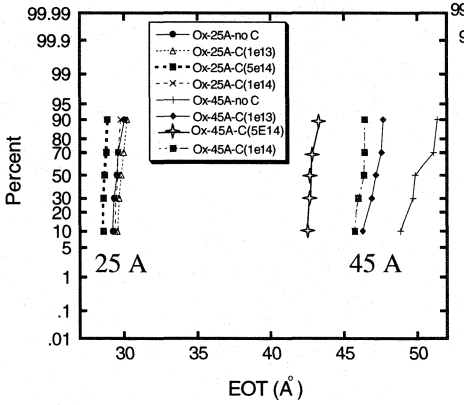

Figure 6: Distribution of EOT for experimental splits

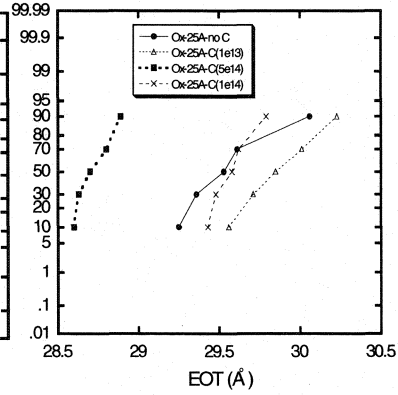

Figure 7: Distribution of EOT for 2.5 nm experimental splits

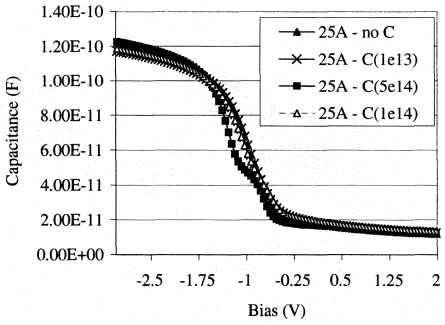

Figure 8: C-V curve (25 A dielectrics)

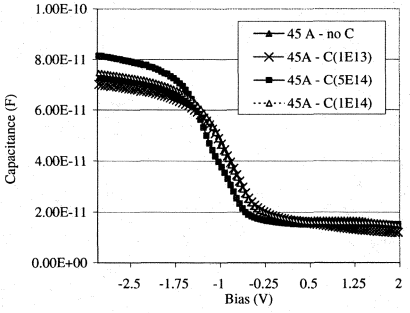

Figure 9: C-V curve (45 A dielectrics)

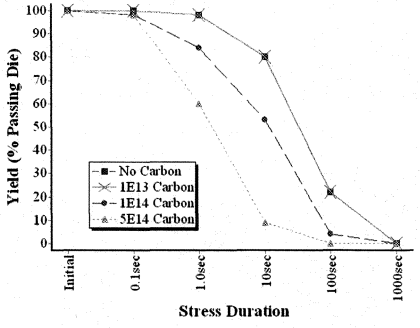

Figure 10: SILC Yield (25 A dielectrics)

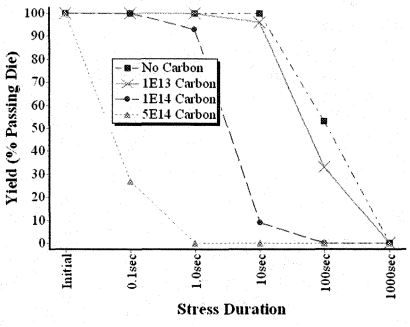

Figure 11: SILC Yield (45 A dielectrics)

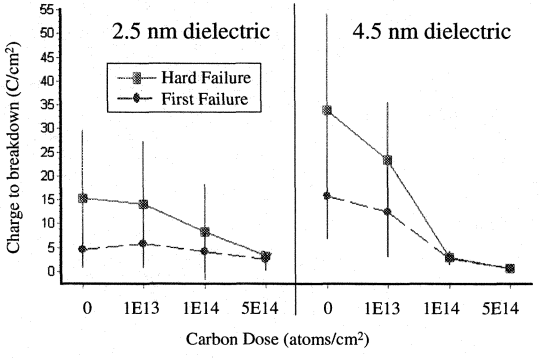

Figure 12: Charge to breakdown

INFLUENCE OF MOLECULAR WEIGHT OF ORGANIC CONTAMINANTS UPON ADSORPTION BEHAVIORS ONTO SILICON SURFACES

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The adsorption behaviors of organic contaminants on wafer substrate surfaces have been investigated. We found the adsorption enthalpy of organic hydrocarbons onto the silicon surface becomes large as the molecular weight (MW) of contaminants increases. Based on these research results, we will explain the influence of the molecular weight of organic hydrocarbons upon adsorption behaviors onto silicon surfaces and suggest a model of adsorption behaviors of various hydrocarbons onto wafers.

INTRODUCTION

Many organic materials are used in clean rooms and with equipment. Almost all of organic materials release many kinds of volatiles (out-gases) such as hydrocarbons, phthalic ester, cyclic siloxanes, and moisture. Therefore, it is a fact that many out-gases, such as moisture or organic compounds frequently existed as contaminants everywhere in a clean room. The out-gases are most likely adsorbed onto a silicon wafer's surface.

Recently, it has become known that organic contaminants on wafer substrate surfaces cause many detrimental effects, such as electrical property degradation, yield losses, and so on [1]. As process temperature for giga scale integrated device manufacturing decreases, to prevent silicon wafer surfaces from organic contamination becomes more important for improving the process yield [2]. Since then, several kinds of reduction methods of organic contaminants have been appli ed at semiconductor fabs, for example, the adoption of chemical filters with active carbons to reduce organic contaminants concentration in a clean room. On the other hand, the mini -environmental process is a new semiconductor manufacturing concept to reduce contamination, and a wafer-carrying pod is a typical mini environmental tool to prevent silicon surfaces from organic contaminants. However, these consist mainly of plastics and even these plastics release organic contaminants themselves. So it is a fac t that being completely free from

organic contaminants is very difficult. Therefore, it is very important to figure out what the mechanism of organic contaminant adsorption onto silicon wafer surfaces is.

We have reported adsorption behaviors with organic contaminants onto silicon surfaces using gas chromatography-mass spectrometry (GC-MS) shown in Figure 1 [3]. In this experiment, a silicon wafer was exposed various hydrocarbons in vessel for 24hours. Figure 1 indicates the comparison of the amount of adso rbed various organic contaminants with different molecular weights (MW) of linear aliphatic hydrocarbons. It was considered that the amount of organic contaminants on silicon surfaces depended on its molecular weight.

In order to further explain the behavior, we continued to study the adsorption behavior of hydrocarbons onto silicon surfaces to determine the enthalpy of organic hydrocarbons onto Si-H and SiO_2 surfaces.

EXPERIMENTAL

Figure 2 shows a schematic diagram for the enthalpy of organic molecules on Si surfaces. Si and SiO_2 surfaces were formed on an electropolished stainless steel tube surface by SiH_4 gas. First, the inner surface of the stainless tube (1/4", 2m) was directly passivated by the Si film that was deposited at 450°C for 48 hours using 100ppm SiH_4 in argon ambiance. Second, in case of forming SiO_2, oxygen gas was supplied to the Si deposited surface at 600°C with a flow rate of 100 cc/min. For Si-H formation, the Si deposited surface was annealed at 400°C [4]. The contaminant was generated from organic compound vaporizer using argon purge gas with the flow rate of 100 cc/min, supplied to the sample tube line, and then detected by atmospheric pressure ionization mass spectrometer (API-MS). The sample line was adjusted at 25, 60, 100, 150 and 200°C, respectively.

Figure 3 shows a typical adsorption property on the flowing time. From the starting of the test, we confirmed that all of the tested hydrocarbon adsorbed onto the silicon surface until the surface was saturated by the hydrocarbon. And then, the hydrocarbon was detected by API-MS. All amounts of the adsorbing hydrocarbon onto silicon surface Q are shown in the following scheme.

$$Q = C \times f \times t \qquad [1]$$

C: The concentration of hydrocarbon added in Ar gas (100ppb)

f: Ar gas flow rate (100cc/min.)

t: Initial detection time of hydrocarbon in Ar gas by API-MS.

In order to find the temperature dependency of the amount of the adsorption, the enthalpy of hydrocarbons onto the silicon surface was calculated using the scheme above.

RESULTS AND DISCUSSION

Figure 4 indicates the dependency of the $C_{14}H_{30}$ and $C_{20}H_{42}$ adsorption

properties on the flow time. When the hydrocarbons were supplied to the Si surface, it was adsorbed onto the Si surface. Therefore, a time lag was observed until it was detected by API-MS. The amount of adsorbed hydrocarbons decreases in accordance with the temperature rise, since the surface was immediately saturated in case of high temperature.

Figure 5 shows the dependence of various hydrocarbon adsorption properties. The temperature of the silicon surface was fixed at 60°C. This figure shows that the detection time of each organic molecule differed and that the amounts of adsorbed hydrocarbons increased while the MW increased. The amounts of adsorbed $C_{10}H_{22}$, $C_{14}H_{30}$, and $C_{20}H_{42}$ onto the Si-H surface were 4.6, 90, and 3600 times respectively for that of C_6H_{14}, respectively. The adsorption of hydrocarbon onto the silicon surface was depended on its MW.

Figure 6 shows the Arrhenius plot of various hydrocarbons onto the Si-H and SiO_2 surfaces obtained. This indicates that the amount of adsorbed hydrocarbons is higher as the temperature decreases and MW increases. The enthalpy of hydrocarbon onto a silicon surface was calculated by each slope. Figure 7 shows the correlation between enthalpy and MW of hydrocarbons. This figure indicates that in each case the enthalpy increases along with the increase of the MW.

Judging from our data, the amount of the adsorbed hydrocarbons with the MW can be determined by the correlation between the vapor pressure of the hydrocarbons and the enthalpy onto the Si surface, not only the vapor pressure of the organics. Figure 8 is the model of adsorption behaviors of hydrocarbon onto wafer surfaces. Molecules with low MW are not adsorbed onto the surface. On the other hand, regarding molecules with high MW, the amount of adsorbed molecule decreased. This is attributed to the enthalpy increase, though the vapor pressure decreases with the increase of the MW, therefore, these molecules are not adsorbed onto the surfaces. Base on our results, we proposed linear aliphatic hydrocarbons with the MW between 170 and 370 should not be used in process surface.

CONCLUSION

In this study, the enthalpy of hydrocarbons onto Si-H and SiO_2 surfaces was experimentally determined. According to the results, it was found that the amount of adsorbed lower molecular weight hydrocarbon onto silicon wafer surfaces gets smaller because the enthalpy gets lower.

On the other hand, it is understandable that higher molecular weight hydrocarbon gets more difficult to volatile because the vapor pressure gets lower. So, the amount of adsorbed higher molecular weight hydrocarbons onto silicon wafer surfaces should be smaller because the existence probability of them in the atmo sphere around the surfaces is lower.

From these results, the influence of the molecular weight of hydrocarbons upon adsorption behaviors onto silicon surfaces is depended on the relationship between the enthalpy onto silicon surfaces and the vapor pressure. Finally, we propose a Model of adsorption behaviors of various organics onto wafer surfaces shown in Figure 8.

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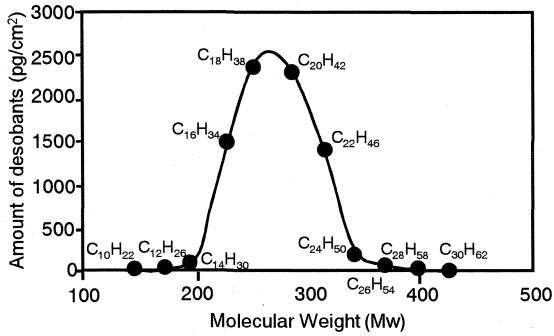

Figure 1. Comparison of the amount of adsorbed various organic contaminants with different molecular weights (MW) of aliphatic hydrocarbons

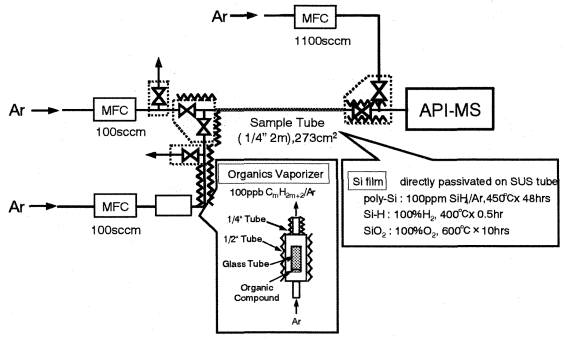

Figure 2. Schematic diagram for the enthalpy of hydrocarbon onto Si surfaces.

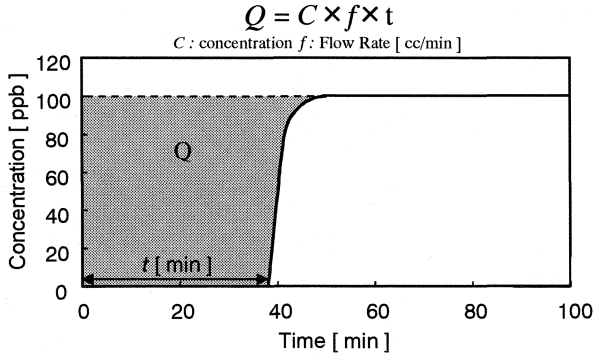

Figure 3. A typical adsorption property on the flowing time

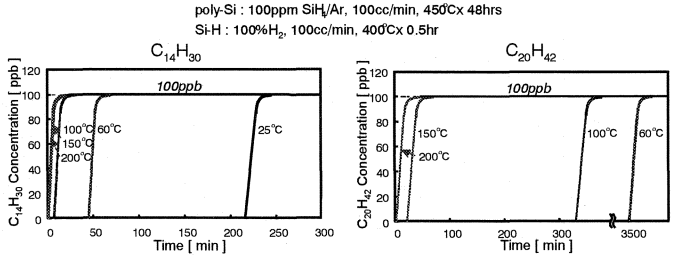

Figure 4. Time dependence of $C_{14}H_{30}$ and $C_{20}H_{42}$ concentration detected by APIMS

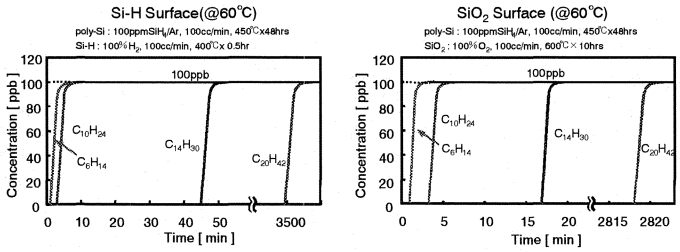

Figure 5. Time dependence of various hydrocarbons concentration detected by APIMS

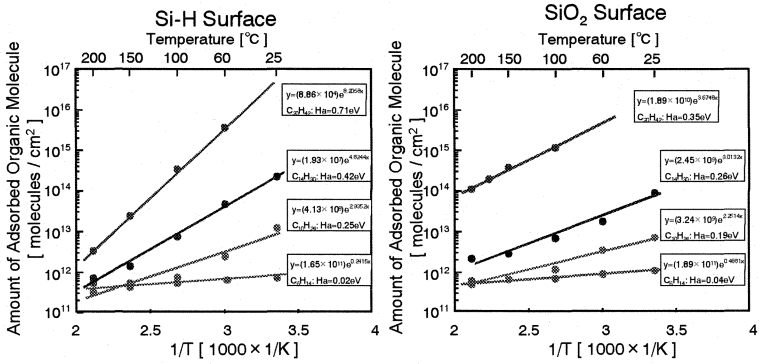

Figure 6. Arrhenius plot of various organic molecules onto the SiH and SiO_2

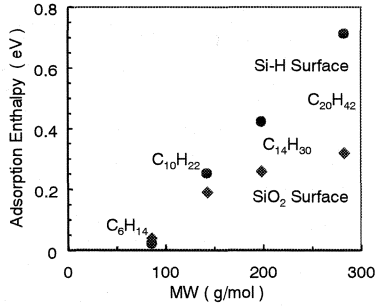

Figure 7 Relationship between enthalpy and MW of hydrocarbon

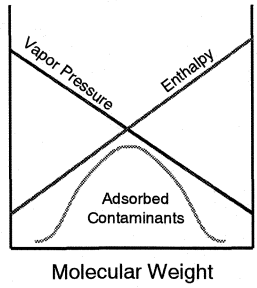

Figure 8. Model of adsorption behaviors of hydrocarbon onto wafer surfaces

THE REMOVAL OF ORGANIC CONTAMINATION BY O_3/DI-WATER PROCESSES: A THEORETICAL STUDY.

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The removal of organic contamination is one of the important cleaning steps during IC manufacturing. Ozone/DI-water processes are more often used as an alternative for the SPM-cleaning concepts to remove this type of contamination from the silicon wafer surface. In order to further improve the efficiency of ozone/DI-water processes, fundamental understanding of the ongoing chemical processes is needed. Therefore a modelling study of the ozone decomposition was initiated to gain insight in the generation of radicals during the decay of ozone in water. With this information reaction parameters can be selected in such a way that either direct or indirect oxidative degradation of organics can be achieved.

INTRODUCTION

The use of ozone in wet and dry cleaning processes of silicon wafer surfaces is a fact these days. In wet cleaning processes, ozonated solutions are used as an alternative for the SPM-cleaning concepts (H_2SO_4/H_2O) and this for various applications, e.g. the removal of organic contamination [1,2,3] and the oxidation of silicon surfaces [4,5,6]. The removal of organic contamination by means of ozone/DI-water is currently investigated thoroughly and this both for contamination originating from the cleanroom ambient [7] as for organic residues from previous process steps (e.g. photoresist). Even photoresist layers of more than one micrometer thickness can be removed by ozone/DI-water [8]. To further improve the efficiency of these cleaning processes, fundamental knowledge on the reaction mechanisms of the removal of organic contamination is needed. In general, the organic contamination can be divided into two classes: saturated and unsaturated organic compounds. For each type a specific reaction pathway is recommendable, namely a radical-based reaction pathway for the saturated organic species (the so-called indirect oxidation) and an O_3-based reaction pathway for the unsaturated species (direct oxidation): Figure 1. Note that the radical species are intermediates formed in the ozone decomposition process.

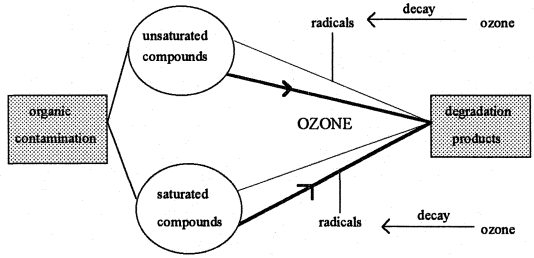

Figure 1: Representation of the two reaction pathways for the removal of organic contamination by ozone in water [8].

The direct oxidation occurs by reaction with ozone itself and it can therefore not be applied to saturated organic species as the rate constant for these reactions is too small to be applicable in semiconductor cleaning processes. The reaction rate constant of these saturated organic compounds with radical species (e.g. the OH-radical) is several orders of magnitude higher than with ozone, thus the indirect oxidation is more recommendable. For unsaturated organic species, e.g. aromatic structures, the reaction rate constant with ozone is comparable to that of radical reactions. Here the direct oxidation is favourable because the ozone concentration exceeds the radical concentration by orders of magnitude. It may be clear that the reaction pathway that has to be chosen depends on the nature of the organic contamination that has to be removed. Reaction parameters of the ozone/DI-water system can be selected in such a way that the appropriate reaction pathway is achieved: a direct or indirect oxidative degradation of the organic species.

OBJECTIVES

When selecting the appropriate reaction pathway, one has to keep in mind two fundamental characteristics of ozone in water: its solubility and decomposition rate in an aqueous solution. The first parameter is important to achieve maximised ozone concentrations in the solution (direct oxidation) and the second parameter determines the generation of radical species. The ozone solubility in aqueous solutions $[O_3]_{liq}$ is already investigated in detail [9,10] and its dependence on pH, temperature and nature of the additive is well documented. The decomposition of O_3 has also been looked at as a function of pH, temperature and nature of the additives [9,11]. To correlate the experimental results with the build-up of radical species in the solution, the ozone decay has to be modelled. In literature two models are often cited, namely the model of Hoigné et al. (HEA) and the model of Gordon et al. (TFG) [12]. Based on these two models which both imply complex radical chain mechanisms, the ozone decay will be simulated using the Facsimile software [13]. By this approach it is possible to gain insight in the radical pathway because the simulations will result in concentration-time profiles of the various

radical species. This information is vital for further optimisation of the silicon surface cleaning processes.

RESULTS AND DISCUSSION

In a first step the ozone decomposition model of Hoigné et al. (HEA) was evaluated at room temperature. This mechanism consists of 32 reactions and 13 different species. First a reduction procedure was performed yielding a reduced HEA-model (RHEA) which only contains 14 reactions and 13 species [12]. Figure 2 shows the essential steps. Among the 13 species involved, the following radical species are withheld: HO_2, HO_3, HO_4, O_2^-, O_3^- and OH. It is known that these radical species are highly reactive, even towards saturated C-C bonds.

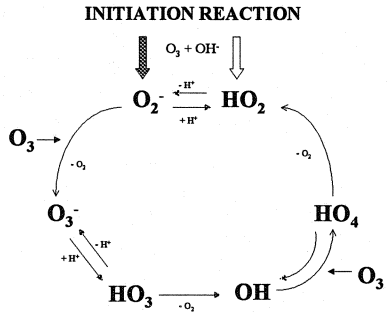

Figure 2: Schematic representation of the ozone decomposition mechanism (RHEA) (the termination steps are not shown on the figure).

The Facsimile software [13] not only simulates the ozone decay (and allows a comparison with experimentally obtained decomposition data [9,11]), but also results in the concentration-time profiles of the radical intermediate species: Figure 3.

As one can see from Figure 3, the concentration-time profiles of the radical species are not all the same: some shown an initial fast build-up to a maximum concentration (C_{max}) followed by a decrease during the ozone decay (e.g. O_3^-) and other radical species reach a maximum concentration at the moment where all ozone has disappeared, namely at t = 7 seconds for pH 7 (e.g. OH and O_2^-).

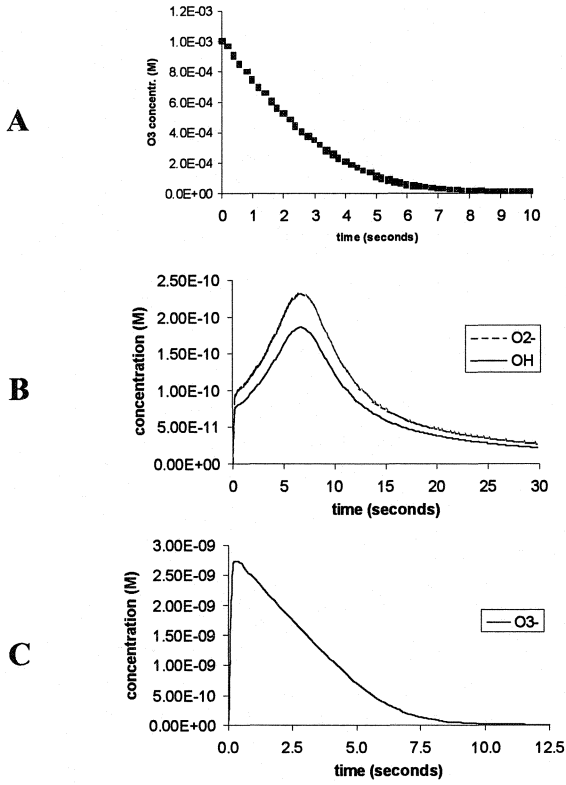

Figure 3: Simulated concentration-time profiles of ozone (A) and some intermediate radicals (B and C) at pH 7 and at room temperature.

As we are interested in the dependence of the concentration of all radical species on pH, temperature and nature of the additive, one can define an additional parameter: the 'Radical Pool' or RP. It is the sum of the maximum concentrations C_{max} of all radicals in the solution ($RP = \Sigma C_{max,i}$). This 'Radical Pool' is clearly dependent on pH as is illustrated in Figure 4. At low pH not only the ozone decomposition is slow [9,11], but also the RP-value remains low. From pH 4 to 5 on, a (fast) increase in RP is observed whereby RP is more than two orders of magnitude larger at pH 7 than at pH 2. There are thus far more radicals present in the solution at near neutral pH than under acidic conditions. Calculations have shown that this trend continues at higher pH-values.

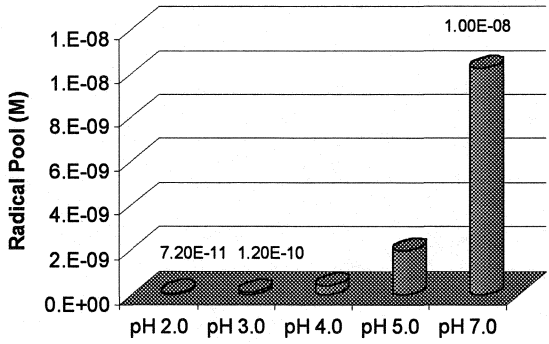

Figure 4: Radical Pool (expressed in mole/l) as a function of pH at room temperature and at initial ozone and oxygen concentrations in the solution of 10^{-3} M: $[O_3]_0 = 10^{-3}$ M = $[O_2]_0$

The dependence of RP on $[O_3]_0$ is also different for acidic and alkaline pH conditions. At low pH almost no dependence of RP on $[O_3]_0$ is observed, e.g. RP is 6.5 10^{-11} M and 7.3 10^{-11} M at 0.5 mg/l and 50 mg/l ozone respectively. At pH 9, RP is strongly correlated with the initial ozone concentration with an increase from 2.7 10^{-8} M at 5 mg/l ozone to 1.1 10^{-7} M at 50 mg/l ozone.

From the above it is clear that for achieving a radical reaction pathway in the removal of organic contamination, one needs to work at near-neutral to alkaline pH-values and high initial ozone concentrations.

Finally the simulations allowed to determine the dominant radical species in the solution at acidic and alkaline pH-values. This strongly depends on the pH as shown in Table I where the relative contributions of the various radicals to RP is given. The most abundant species at low pH is the HO_2-radical and the O_3^--radical at a pH of 9.

One sees that the HO_2 and O_3^- radicals are the most abundant species at respectively pH 2 and 9.

It should be noted here that the OH-radical is only of minor importance and probably does not play a major role in the degradation of organic contamination.

Table I: Relative contribution to the RP of the radical species (%) at pH 2 and 9 and $[O_3]_0 = 10^{-3}$ M.

	pH 2	pH 9
HO_2	89.8	1.6
HO_3	2.0	2.3
HO_4	7.9	8.8
O_2^-	0.10	1.0
O_3^-	$4\ 10^{-4}$	85.4
OH	0.11	0.8

Future research includes the search for correlations between the ozone cleaning and oxidising efficiency with the magnitude and the composition of RP at various experimental conditions such as pH, initial ozone concentration and temperature. The removal of organic contamination from silicon wafer surfaces and in process rinse waters will be investigated both by experimental work and by modelling. Also the effect of the addition of ozone decomposition promoters and scavengers will be looked at.

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REMOVAL OF LIGHT AND HEAVY ORGANICS BY OZONE PROCESSES

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Organics adsorbed onto the wafer surface cover a large range of compounds and are classified in two broad classes: heavy organics (photoresists and post-ash residue) and light organics (all other organics that are *not* heavy organics). In this work, a method is presented to show the uniformity of light organic removal from the wafer surface by an ozonated DI water process. A bare silicon wafer was coated with a challenge organic (hexamethyl disilazane; HMDS) which was then removed by ozonated DI water. Contact angle measurements and AFM scans of the post process wafer showed a clean, organic free wafer surface with no HMDS islands. The difference between light and heavy organic removal is discussed with emphasis on the theoretical requirements for a heavy organic removal process. Hardware challenges for a heavy organic cleaning process are discussed and preliminary resist strip rates are presented.

INTRODUCTION

Volatile organics can adsorb on silicon wafers in clean rooms and introduce severe defects during semiconductor manufacturing steps [1]. The volatile organics that adsorb on silicon wafer are classified differently from photoresist and resist residues left on the wafer surface after ashing. The latter are defined as heavy organics while the volatile organics are defined as light organics. In other words, any organic contaminants on the wafer that are not resists or resist-residue are defined as light organics [2].

Typically, organics (light and heavy) are removed from a wafer surface in a sulfuric acid and hydrogen peroxide mixture (SPM) at high temperatures. This is an aggressive chemistry as it mixes concentrated sulfuric acid (98 wt%) with hydrogen peroxide (31 wt%) in a 4:1 ratio [3]. High temperatures (120 ^{o}C or more) are needed for the SPM to be effective with periodic additions of hydrogen peroxide. While the SPM process can remove any type of organic from the wafer surface, the process is expensive in terms of chemicals and DI water usage. It also reduces the wet process equipment life and introduces metal and inorganic contaminants such as sulfate onto the wafer surface.

With emphasis on reduced cost of ownership and improved performance, removal of light organics by ozonated DI water has been proposed. It is a reduced consumable cost process that has fewer processing steps and is carried out at room temperature with

minimal environmental impact. Because hydrogen peroxide is not used, metal contamination is significantly reduced in a dissolved ozone process. Particle additions are reduced in an ozonated DI water process as well [4-6]. Because of these advantages, light organic removal by ozonated DI water is increasingly being used in the industry.

In this work, a combination of a simple technique (contact angle measurements) and an advanced surface analytical technique (atomic force microscopy, AFM) has been used to assess the uniformity of the light organic cleaning process. These methods provide information on the macro level (contact angle measurements) and at the molecular level (AFM imaging of the wafer surface provides a visual observation of light organics) to characterize the complete removal of light organics. The results from both of these measurements will be used to show the complete removal of light organics from the wafer surface using a single pass of ozonated DI water.

In order to demonstrate the effectiveness of the ozonated DI water clean, wafers were coated with a challenge light organic material (hexamethyl disilazane, HMDS) and were then cleaned using a single pass of bubble-free ozonated DI water. HMDS is commonly used as a photoresist adhesion promoter and is a difficult organic residue to remove from a silicon oxide surface [7]. Removal of HMDS by various cleaning chemistries was used as a process benchmark for light organic removal by many researchers in the past [4,7-10]. The reaction between HMDS and the surface silanol groups results in the formation of a trimethyl siloxane, TMS, monolayer on the wafer surface (Figure 1). It is the TMS layer that is the challenge light organic layer; attack of the TMS layer by ozone restores the silanol termination on the wafer surface. The reaction between HMDS and the surface silanol groups is written below:

$$(CH_3)_3\text{-Si-NH-Si-}(CH_3)_3 + 2(\text{Si-O}^-\text{-H}^+) \Leftrightarrow 2(\text{Si-O-Si}(CH_3)_3) + NH_3 \qquad (1)$$

In this work, light organic removal from the wafer surface was characterized by contact angle and AFM measurements using a simple method. The difference between light and heavy organic removal is discussed with emphasis on the theoretical requirements for a heavy organic removal process. Hardware challenges for a heavy organic cleaning process are discussed and preliminary cleaning results are presented.

EXPERIMENTAL

Prime silicon wafers (200 mm, boron doped p type, 100 orientation, CZ grown) were used in the light organic removal study. A simple method, as outlined in Figure 2, has been established to further characterize the light organic removal using AFM. The native oxide was stripped with HF and an ozone passivation oxide grown in its place. After being vapor deposited with HMDS, the wafer was cleaned using either a SPM bath or ozonated DI water. The oxide on the wafer surface was etched in HF to produce a contrast between the bare Si surface and any post-process remaining HMDS on the wafer

surface. An AFM analysis of the wafer surface was then done to verify complete removal of the HMDS.

Contact angle measurements were made using a Krüss goniometer. Ozonated DI water was generated using a Liquozon 100 system (ASTeX, Wilmington, MA). A flow rate of 5 liters per minute, a process time of 10 minutes and a single pass of ozonated DI water were used to remove the light organics. AFM measurements were done using Dimension 5000 and Nanoscope IIIA atomic force microscopes (Digital Instruments, Santa Barbara, CA) in both the tapping and force modes.

For heavy organic removal experiments, Shipley DUV 6 photoresist was blanket coated on 200 mm wafers. The DUV photoresist was deposited to a thickness of 7500 Å, step baked at 110 and 160 °C and stabilized with an UV lamp to cross link the photoresist. Ozone gas was generated using a SEMOZON 90 generator (ASTeX, Wilmington, MA).

The heavy organic removal process used is a proprietary process involving ozone gas, ozonated DI water and water vapor. All the cleaning and etching experiments were carried out in a commercial automated wet bench (SCP Global Technologies, Boise, ID).

RESULTS AND DISCUSSION

Light Organic Removal

Pre- and post- ozone process contact angle measurements indicated complete removal of HMDS from the wafer surface as shown in Table I. AFM scans were done on wafers subjected to the test procedure outlined in Figure 2. This method allows for an AFM image to reveal any light organic not removed in the cleaning process at the molecular level. This method is specially useful when facilities to measure electrical properties of the wafer are not available. In summary, this procedure is a short loop process sequence to provide fast feedback on the cleaning process.

The AFM images shown in Figure 3 (a) are typical of a clean wafer surface and these results clearly indicate the absence of any light organic residue left over after the ozone cleaning process. In contrast, Figure 3(b) shows an AFM scan of a HMDS monolayer on the wafer surface. It is a very roughened surface with peaks, ridges and partial caldera rims visible over the entire surface. None of these are visible in Figure 3(a) showing the complete removal of the HMDS by the ozonated DI water. The uniformity of light organic cleaning, at the molecular level, is further demonstrated by the sub-Angstrom rms surface roughness measured (Table I) on these wafers after the removal of challenge organic materials.

Differences Between Light And Heavy Organic Removal

Some of the main differences between light and heavy organics are summarized in Table II. While removal of both types of organics is critical in obtaining a pristine

surface for the next processing step, removal of heavy organics is far more challenging. This is because the heavy organics are present in much larger amounts on the wafer surface and should take a longer time for the same removal chemistry. In addition, heavy organics may have undergone processing steps such as implantation (produces a hard crust on the wafer surface that is difficult to remove) or baking (cross-links the photoresist) or may have been created in very severe conditions (such as post-ashing residues). So immersion of the wafers in an overflow bath containing a small amount of ozone dissolved in DI water may completely remove light organics [4-6], but a similar approach fails miserably for heavy organics for the reasons discussed above. Ozone dissolves the photoresist layer by layer so the presence of a hardened crust slows the heavy organic removal down considerably. Given that one can dissolve only a hundred ppm of ozone or so in water and that tens of thousands of ppm of ozone are available in the gas phase, theoretical and experimental results [11] verify that vapor phase ozone processes are the obvious choice for heavy organic removal.

Critical Factors Affecting Heavy Organic Removal by Ozone

Since heavy organics are polymeric in nature, higher processing temperatures will swell, soften and/or breakdown the intra- and inter- chemical bonds in the polymer chains. Higher process temperatures are expected to increase the kinetics of the ozone attack of the heavy organic as well. This has been experimentally observed by many research groups [5,6,11,12].

A synergistic effect of water is also found to increase the heavy organic rates of attack by ozone [11,12]. However, too much water injection during the vapor phase process allows for condensation of water on the wafer and leaves photoresist intact beneath the condensed water. Therefore, an optimum amount of water needs be used in the process.

As ozone is one of the reactants in the heavy organic removal process, increasing its concentration in the tank will only increase the rates of heavy organic attack by ozone. This can be done by delivering more ozone to the tank or by additives that help maintain ozone concentration by reacting with the OH* radical (produced during indirect breakdown of ozone) and preventing any further chain breakdown of ozone. However, it would be more beneficial to have an additive that attacks the photoresist than one that maintains ozone concentration. Attack of the implanted crust by the additive would result in a much larger increase in the rates of heavy organic attack by ozone.

Hardware Challenges for a Heavy Organic Process Chamber

All the critical factors discussed above need to be optimized in order to obtain reasonable PRS rates. Unfortunately, designing a process chamber to accomplish an optimized process is not trivial. While its high reactivity makes ozone a powerful oxidizing agent, requiring ozone in tens of thousands of ppm in the heavy organic chamber at elevated temperatures causes ozone to attack a wide range of materials used in chamber construction and makes it a severe ESH hazard that needs to be contained.

For example, an environment of > 10 ppm of ozone is an IDLH (immediately dangerous to life and health) hazard. So ozone needs to be safely and quickly exhausted from the process chamber (that contains tens of thousands of ppm of ozone) into an ozone destruct. This is countered by the need to ensuring sufficiently long residence times of ozone gas in the tank to attack the heavy organics. Also an adequate number of ambient ozone safety monitors need to be placed at various locations around the process chamber and/or the ozone generator to detect any ozone leaks.

In addition, high process temperatures have to be maintained in the chamber despite the condensation of water on the wafer and chamber walls and the introduction of room temperature ozone gas. This requires providing sufficient thermal energy to the wafer and chamber while making sure that the ozone gas and any additives used in the process are selectively attacking the heavy organics and not the materials used to construct the chamber. These factors require careful optimization of the flow distribution of ozone gas, water vapor and ozonated water.

Based on the considerations listed above, a heavy organic process chamber has been built and preliminary test results obtained. The heavy organic removal process used is a proprietary process involving ozone gas, ozonated DI water and water vapor. Stripping rates of heavy organics from wafer surfaces were found to be accelerated by using an optimum amount of water, high ozone gas concentration using additives and high process temperatures. Initial test results indicate a strip rate of 700-800 Å/min. for a hard baked, cross-linked DUV 6 photoresist. Further testing is in progress with a strip rate goal of 2500 Å/min. PR stripping rates and results of continued optimization of the factors discussed above will be presented at a later date.

SUMMARY

Light organic removal from the wafer surface by ozonated DI water was characterized by a combination of contact angle and AFM measurements. This method provides a quick confirmation of the effectiveness of light organic removal before the electrical results are obtained. Results from the characterization methods used in this work clearly indicate that the ozonated DI water process is capable of replacing the SPM bath for light organic removal. Differences between light and heavy organic removal was discussed with emphasis on the critical factors affecting the heavy organic removal process. Hardware challenges for a heavy organic process chamber were also discussed.

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Table I Contact angles and surface roughness of silicon wafer under different conditions

Sample	Contact Angle*	RMS Roughness
Silicon wafer with HMDS monolayer	76 ± 1°	3.39 Å
Silicon wafer after HMDS strip by ozonated DI water	< 10°	7.27 Å
Silicon wafer after HMDS strip by SPM	< 10°	0.92 Å

* Average of 25 points over the wafer surface

Table II A comparison of heavy and light organics

Light Organics	Heavy Organics
Generally present as a sub-monolayer, monolayer or few layers in thickness (3 to 20 Å)	Photoresists are present as many layers (a few thousand to tens of thousands of Ångstroms in thickness) Post-Ash residue(s) are less than a monolayer in thickness
Unintentionally adsorbed on wafer surface. Adsorbed layer maybe partial or complete depending upon the wafer's exposure to the light organic(s) source Viewed as contaminant on wafer surface.	Photoresists are intentionally deposited on wafer surface for masking parts or the entire wafer surface Photoresist processing may require implantation resulting in formation of highly carbonized, cross-linked surface layer that may be a few hundred of Ångstroms in thickness Post-Ash residue(s) are created as a by-product of the ashing step
Can be completed removed in a furnace at 400 °C. Easily removed by a single wet processing step	Thermal removal at 400 °C not possible Require much more aggressive removal chemistries; some heavy organics may require a dry and a wet processing step

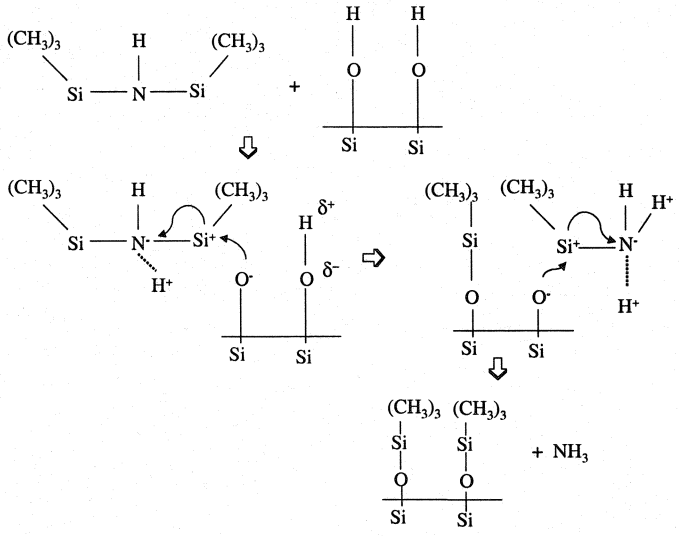

Figure 1. HMDS bonding mechanism with a hydrophilic Si wafer surface (from ref. 4)

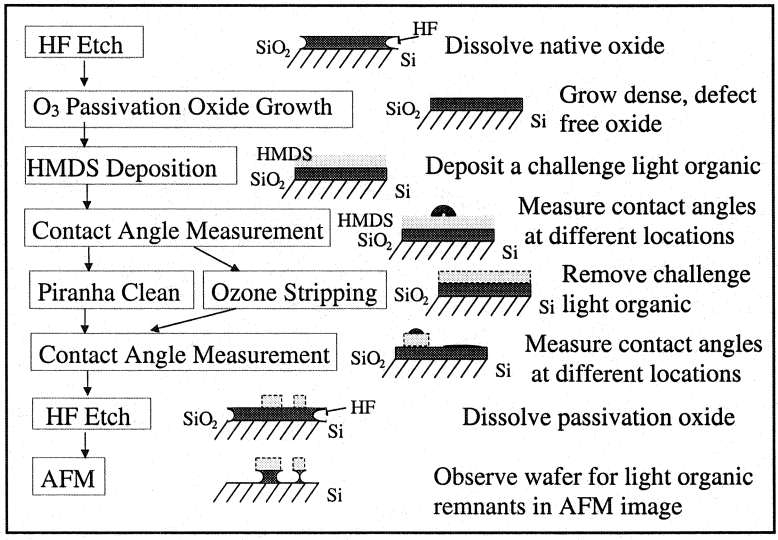

Figure 2. HMDS test plan showing the changes taking place at the Si surface corresponding to the various processing steps in the plan.

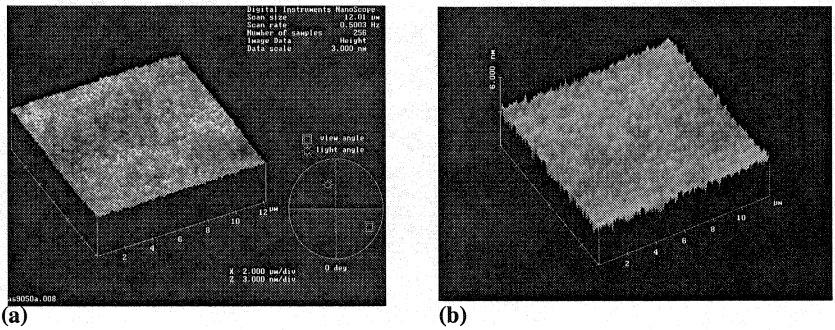

Figure 3. Typical three-dimensional AFM scans of wafer shown in Figure 2. (a) after ozonated DI water cleaning and (b) after HMDS priming and before stripping. Note the 30 Å z scale in 3(a) and the 60 Å z scale in 3(b) showing the much smoother surface in 3(a).

EFFECT OF pH VALUES IN OZONIZED ULTRAPURE WATER ON CLEANING EFFICIENCY

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We have investigated the effect of pH values in ozonized ultrapure water (O_3-UPW) on cleaning efficiency. The metallic removal efficiency from the surface has a big difference with the times. Even though the O_3-UPW is well known to chemicals with the impurity removal efficiency, the cleaning on the surfaces with delaying time after contamination is not effective in our study. The strong relationship between metallic removal efficiency and pH and oxidation-reduction potential (ORP) values in solution is also clear when examining an O_3-UPW cleaning. The cleaning with a pH 4 can remove the metallic impurities below 10^{11} atoms/cm^2 which are just existed in or on native oxide. Still more, the organic removal efficiency of O_3-UPW with pH value of 4 is best superior to that of other cleanings.These results lead to the conclusion that acid added to O_3-UPW is very effective for removal of metallic impurities and organic contaminants.

INTRODUCTION

With down scaling of ultra large scale integrated (ULSI) devices, contamination-free Si surface is essential to realize the high performance of devices since contaminants cause electrical defects, device degradation and yield losses. Now, the time will soon come when the semiconductor industry is required to manufacture the superfine pattern of less than 0.13 microns on 12 inches wafers. Extended conventional technology just as yet, factory scale is very hypertrophied, and semiconductor industry can not advance steadily. It is very important to simplify wet cleaning processes in terms of productivity, energy

saving and cost performance. The cleaning method that in 1970 was proposed by Werner Kern of the RCA Company (the so-called RCA cleaning)[1] has been largely used in the semiconductors processes for a quarter of century and it is still. However, the RCA cleaning process uses chemicals and ultrapure water (UPW) in large volume at high temperature. As a result, it generates a huge amount of chemical vapor that requires the use of a large amount of exhaust capacity to separate cleanroom air from chemical vapors. Therefore, to remove chemical components from exhaust air, the load on the scrubbers is also raised. As chemicals and UPW are evaporated in large volume, the chemical composition of the cleaning solution can not be maintained at a constant level, which inevitably deteriorates accuracy and re-producibility of the cleaning process. The most important issue for mass production is that all cleaning processes have high re-producibility at anytime. In order to suppress chemical vapor generation from wet stations, wafer surface cleaning should be carried out at room temperature, conclusive. Several requirements for future wet cleaning technology should be satisfied for developing an effective cleaning technology, which are; 1) room temperature process, 2) reduction in process steps, 3) reduction in chemical and UPW consumption, and 4) system footprint reduction [2], [3]. We scholarly clarified the mechanism of the removal of the adhered contamination such as metallic impurities, particles and organic. At the base of the mechanism, we propose room temperature wet cleaning process that consists of only 4 process steps in this article.

The 4-step room temperature cleaning reveals a drastic reduction of chemical and UPW use as well as promotion of ESH (Environment, Safety and Health) in semiconductor manufacturing, and clearly indicates that using the room temperature cleaning process to replace conventional RCA cleaning yields equivalent or better cleaning performance for all impurities. A small amount of specific gases dissolved in UPW such as O_3-UPW and NH_3 added to hydrogenated ultrapure water (H_2-UPW) based on cleaning target is only used for wafer surface cleaning. Compared to RCA cleaning, no chemical vapors are generated during the process because cleaning is been processed at room temperature and the cleaning solution is based on very dilute chemicals. In the 4-step cleaning, fresh liquids are continuously supplied but with low-cost and high-performance. This eventually will meet the requirement for coming severe cleanliness, larger diameter wafer processing and greater respect for the environment.

The O_3-UPW with the economic benefits became to play an important part in current wet cleaning [4]. However, the cleaning efficiencies for removing contaminants such as noble metals and organic contaminants, and etc, should be much improved, compared to those of typical cleanings [5]. The present work focuses on an effect of pH values in O_3-UPW on cleaning efficiency in great detail.

EXPERIMENTAL

Two types of crystalline silicon (c-Si) wafers used were type A [8-in. p-type (100) oriented wafers with resistivity of 10 Ω·cm] and type B [8-in. n-type (100) oriented wafers with 3 to 5 Ω·cm]. The samples are pre-cleaned by a sequential cleaning of sulfuric

acid-hydrogen peroxide mixture (SPM: 4:1, 90°C) for 10 min., a 0.5% HF for 30 sec., and post ultrapure water (UPW) rinse with a resistivity of 18.2 MΩ·cm for 10 min.

In order to investigate the removal efficiency of metallic impurities and organic contaminants, the wafers are contaminated using various contaminants. Following, these contaminated wafer surfaces were cleaned in pH controlled O_3-UPW. In every cleaning process, the cleaning time was set to 10 min. and dried with ultrapure nitrogen gas.

The amount of deposited metallic impurities is analyzed with an incident angle of 0.05 degree by Total Reflection X-ray Fluorescence Spectroscopy (TRXRF) system using W x-ray source of 30 kV and 200 mV.

The amount of organic contaminants is determined by use of fourier transform infrared reflectance-attenuated total reflection (FTIR-ATR) with germanium as a prism material. The hydrocarbon signals from the Si surface are observed around the wave number of 2900 cm^{-1}.

RESULTS AND DISCUSSION

Figure 1 shows the dependence of copper (Cu) removal efficiency of O_3-UPW on exposing time in cleanroom after contamination. The Cu concentration in the contamination solution was set to 1 mg/l Cu using $CuCl_2$ in UPW with a resistivity of 18.2Ω·cm for all dipping solutions. Then the samples were exposed at cleanroom air. Cu removal efficiency from surface has been found to be totally different as a function of exposure time. O_3-UPW cleaning is not efficient on Cu impurity removal when samples after contamination are stored for long time, while Cu impurity on surface is easily removed when no delay takes place after contamination [6].

Figure 2 compares the x-ray photoelectron spectroscopy (XPS) spectra of the Cu contaminated Si surfaces. Judging from the ghost peaks on increasing exposure time, the surface of contaminated copper seems to be oxidized more and more. We point out that the surface oxidation on the Cu strongly affects the removal efficiency of the cleaning method. That is, the O_3-UPW with a high oxidation-reduction potential (ORP) value doesn't have the capability to remove the oxidized Cu impurities from the surface. This is attributed to the pH value of the solution, which has almost neutral pH value of 6.5: close vicinity to phase boundary of Cu ions and CuO in solution. It is therefore mandatory to decrease the pH value to improve the impurity removal efficiency from substrates.

Figure 3 shows the dependence of etch rate of Cu and CuO films on various chemical concentrations in UPW. CuO film in acidic solutions with a low pH value has a fast etch rate, while Cu film is not etched in all concentrations. CuO film can be only dissolved to Cu^{2+} ions in solution with a high ORP and low pH value. Therefore, authors suppose that an acidic solution is added to O_3-UPW to decrease the pH value, so that all Cu compositions such as metallic Cu, Cu oxide, and Cu hydroxide can be removed from silicon substrate. When adjusting pH value in O_3-UPW, ORP values are in total accord irrespective of the species of acidic solutions. However, It is reported that Cl ion residues promote Cu adsorption on substrate at the post cleaning step and particle generation during next deposition [7]. This is because stable states of silicon surface are partially

replaced by active states of Cl termination. According our results, since CO_2 added O_3-UPW does not remain chemical residues after cleaning, we replace HCl with CO_2 in O_3-UPW.

Figure 4 represents the influence of pH and ORP values in the solution on the removal efficiency on Cu contaminated silicon surfaces, which were exposed in cleanroom ambiance after contamination for 2 days. The pH value of the solution was controlled by method of adding CO_2 to O_3-UPW. CO_2 in the O_3-UPW was dissolved with a hollow fiber type membrane. The strong relationship between removal efficiency and those values in solution is also clear when examining an O_3-UPW cleaning. After O_3-UPW cleaning with a pH 4, Cu impurities on silicon substrate are below 10^{11} atoms/cm^2, which are just existed in or on native oxide.

Figure 5 shows the removal efficiency of organic contaminants with various cleaning solutions. The amount of organic contaminants is determined by use of a fourier transform infrared reflectance-attenuated total reflection (FTIR-ATR) with germanium as a prism material. The hydrocarbon signals from the silicon surface are observed around the wave number of 2900 cm^{-1}. The removal efficiency of new CO_2 added O_3-UPW is best superior to that of other cleanings.

Figure 6 is showing the pH and ORP values of various solutions. In general, the ORP values in solutions increase with the decrease of pH value at same solution. The O_3-UPW has much high ORP value on adding CO_2 to the solution. The increase can affect the organic contaminants removal from Si surface (fig.5). Based on our results from metallic impurities and organic contaminants removal from wafer surface, we propose CO_2 added O_3-UPW instead of O_3-UPW only, so that, the 4-step room temperature cleaning is changed into Table 1;

1st step: CO_2 added O_3-UPW cleaning for removing of organic and metallic impurities.
2nd step: NH_3 added H_2-UPW + Megasonic (MS) cleaning for removing of particles.
3rd step: FPM cleaning for removing of metallic impurities.
4th step: H* radical added UPW rinse for removal of chemical residues, prevention of particle re-adhesion, suppression of native oxide growth, and enhancement of H-termination.

The room temperature cleaning, based on the pH controlled O_3-UPW, can be easily applicable for the state-of-art cleaning.

CONCLUSION

We have investigated the effect of pH values in O_3-UPW on cleaning efficiency. An O_3-UPW cannot remove surface oxidized copper particles, even though it has high ORP value. In order to remove all copper impurities on Si surface irrespective of contaminated conditions such as metallic Cu, Cu oxide, and Cu hydroxide, therefore, the pH value of O_3-UPW should be controlled less than 4. Still more, the organic removal efficiency of O_3-UPW with pH value of 4 is best superior to that of other cleanings.

A pH controlled O_3-UPW (CO_2 added O_3-UPW) is newly added to 4 steps room temperature cleaning, resulting in improving the removal efficiency of copper impurities and organic contaminants. The room temperature cleaning based on using pH controlled functional water is a good candidate for future cleaning in this article.

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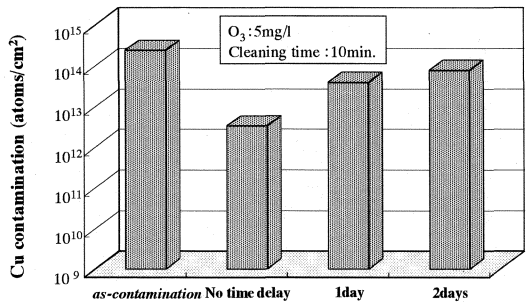

Fig.1. The dependence of Cu removal efficiency of O_3-UPW.

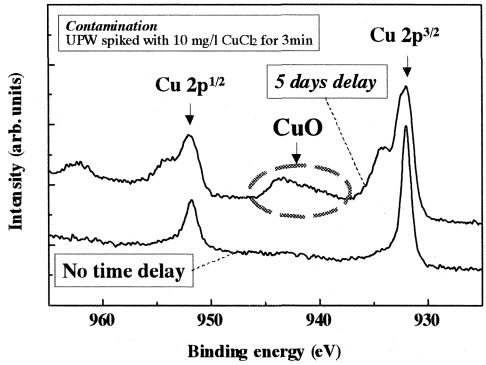

Fig.2. XPS spectra of Cu contaminated silicon surface on exposing time in cleanroom.

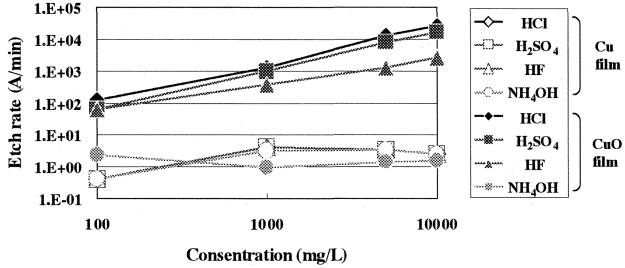

Fig.3. The dependence of etch rate of Cu and CuO films on various chemical concentration s in UPW.

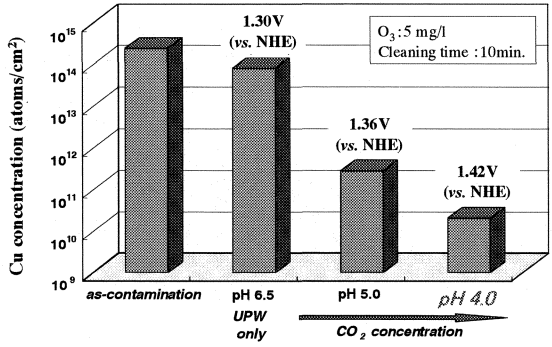

Fig.4. The dependence of Cu removal efficiency on pH and ORP values in CO_2 added O_3-UPW.

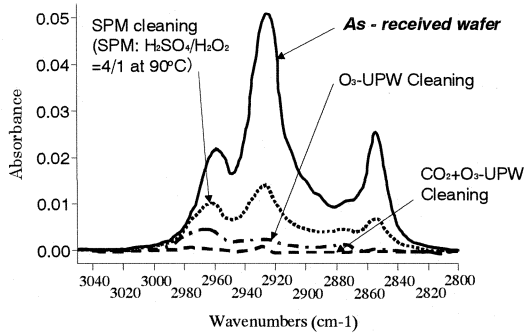

Fig.5. FTIR-ATR spectra of remaining hydrocarbon on silicon surface.

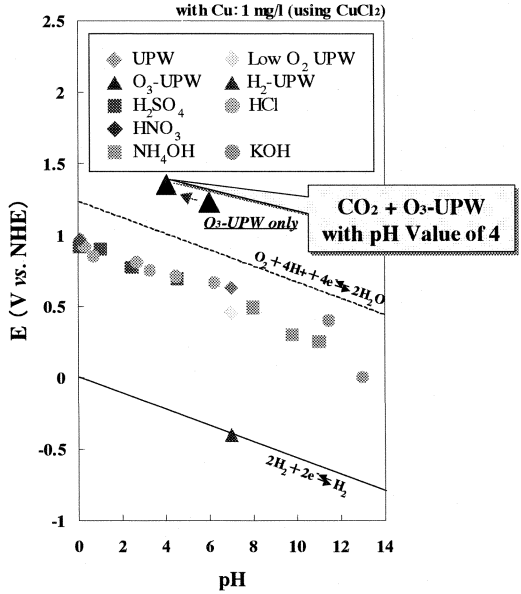

Fig.6. pH and ORP values of various solutions.

Target	Cleaning Sequence
Organic Metal	CO_2 + O_3-UPW (pH=4.0)
Particle	NH_3 + H_2-UPW with MS（pH=9.3-10.0）
Metal	FPM (HF/H_2O_2)
Rinse	H· Radical added UPW

(MS : Megasonic)

Table 1. 4-step room temperature wet cleaning.

REMOVAL OF PHOTORESIST BY O_3/DI-WATER PROCESSES: DETERMINATION OF DEGRADATION PRODUCTS

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ABSTRACT

Since a few years the use of O_3/DI–water processes in photoresist (PR) removal is under investigation. This work reports the determination of the most important degradation products formed after the stripping of two different types photoresist (I-line and DUV) by ozone processing.
From the obtained experimental data, it was clear that the largest fraction of carbon present in the photoresist is converted to organic compounds in the process water. Samples of this process water were analyzed with Ion Chromatography and Headspace GC-MS techniques. Twenty different compounds were identified as degradation products for the I-line resist and eighteen compounds for the DUV resist. Carboxylic acids were found as the most important degradation products. A large fraction of the organic carbon in the process water could not be identified with the used analytical techniques.

INTRODUCTION

Organic contamination in IC-manufacturing is characterized by a large number of sources and a large variety of chemical structures of the contaminants. Concerning this organic contamination a distinction can be made between two groups. The first class includes these organics which adsorb from the environment on the substrate[(1)]. Main sources of these contaminants are the clean room air, clean room construction materials, wafer storage and shipping materials. Important contaminants are for example additives (sensitizers, anti-oxidants, flame inhibitors,...) in plastic materials[(2)]. In the second class organics are implied which originate from the IC-processing itself.
One of the most important sources of this latter organic contamination is the photolithographic process. After each photolithographic step, remaining photoresist residues must be completely removed from the silicon surfaces or otherwise they lead to organic contamination. Since a few years, the application of ozonated DI-water (De-Ionized) for the removal of PR residues is under study [(3,4,5,6,7)]. These processes form an alternative for the sulfuric acid based stripping solutions like SPM and SOM[(8,9)], and they

combine an effective cleaning with a lower cost of ownership. The strength of these ozone based processes is that ozone dissolved in water is characterized by a very high redox potential and therefore is likely able to oxidize all types of organic material.

The aim of the performed experiments was to determine possible degradation products which are formed in the removal of photoresist material by ozonated processes. The identification of these compounds generates valuable information for a fundamental understanding of the oxidative degradation of photoresist material by ozone in ultra pure water. Also it is hoped that identification and quantification of the organic loading of the process water will allow efficient regeneration and re-use of the rinse water.

EXPERIMENTAL

Batches of 24 wafers were coated with two different types of photoresist: I-line IX 845 resist and DUV TOK022 resist. For the I-line resists a standard thickness of about 1200 nm is applied to the wafers while for the DUV resist it was about 650 nm.

For the PR stripping a Spray Acid Tool (SAT) from Semitool, equipped with an ASTEX AX8400 ozone generator, was used. The tool consists mainly out of a heated process chamber in which a cassette of wafers can be placed. During processing, the chamber is saturated with ozone and the wafers are rotated under continuous spraying of water. With this technique, a thin "boundary" water layer is maintained on the wafer surface and the process water is recirculated through a reclaim tank[10].
The overall process includes a stripping, rinsing and drying step and lasts about thirty minutes. The temperature of the DI-water was 85°C and no additives were added. The gas phase ozone concentration was approximately 185 g/m^3. Samples were taken from the reclaim tank and analyzed. The sampling sequence is presented in Figure 1.

Fresh water in the reclaim tank
↓ ↳ Blank
Stripping full batch of I-line wafers
↓ ↳ Sample I-line
Fresh water in the reclaim tank
↓ ↳ Blank 2
Stripping full batch of DUV wafers
↓
Stripping a 2nd full batch of DUV wafers
↳ Sample DUV

In a first step, a tool blank was taken from fresh water in the reclaim tank. After the stripping of a batch of I-line resist coated wafers, a first sample was taken. The water was drained and after refilling the reclaim tank with fresh DI water a second blank was taken. Then two batches of DUV wafers were stripped and after the stripping of the second one, a sample was taken. Between the two stripping processes, the process water remained in the reclaim tank.

Figure 1: Sampling procedure

The samples were analyzed with a Sievers 820 TOC analyzer. This tool measures the Total Organic Carbon (TOC) and Total Inorganic Carbon (TIC) content in the samples

(expressed in ppm). The samples were subsequently analyzed with Ion Chromatography (I.C.) and Dynamic Headspace GC-MS (HS GC-MS).

For the I.C. analyses, a DX 500 tool from Dionex was equipped with an AS11-HC analytical column preceded by an ATC column and a GS11 guard column. An ASRS I suppressor unit and a CD20 conductivity detector were used. For sample analysis, a gradient elution method is used with DI water, a 10 mM and 100 mM NaOH solution as eluents. These eluents were freshly prepared every day and stored in a polyethylene flask. The column pressure was always between 1700 and 1800 psi, the flow rate of the eluens was 0.38 mL/min. and the suppressor current 100 mA.

Headspace analysis was performed at DCMS (Development Center for Chromatography & Mass Spectrometry) in Bierges, Belgium. The samples were analyzed with a Tekmar LSC2000 Purge and Trap system coupled to a Fisons MD 800 GC-MS, according to a method based on the EPA 524.2 protocol.

RESULTS AND DISCUSSION

TOC After the PR stripping of 1 batch of I-line wafers, a TOC of 35.15 ppm and a TIC of 3.57 ppm was measured in the process water (Sample I-line). After striping two batches of DUV resist a comparable TOC of 33.15 ppm was measured. The TOC content in both blank samples (Blank I-Line, Blank DUV) was very low (below 50 ppb), typical for DI-water.

Calculations In order to investigate the PR stripping process quantitatively, an approximate calculation of the amount of carbon present in each batch PR wafers was made and compared with the experimental TOC and TIC data.
In a first step the total mass of photoresist ($m_{(PR)}$) in a full wafer batch was calculated using equation (1):

$$\mathbf{m_{(PR)}} = \rho \,.\, \Sigma_i \,(\Pi \,.\, \mathbf{R^2}) \,.\, \mathbf{d_I} \qquad (1)$$

with ρ the density of the PR-layer in g/cm^3 and (Σ_i (Π . R^2) . d_i) the total volume PR in the batch. The latter is given by the sum of the PR volume on each wafer (**i** = 24), **R** the radius of the circular PR layer, and **d** the thickness of the PR layer each in cm. The value of **R** was 9.74 cm and **d** was determined with a Spectramap 3400 ellipsometer.

Values of PR layer densities were estimated to be between 1.0 and 1.2 g/cm^3 [11,12,13,14] and our calculations were made with these two limit values.
From the calculated value of $\mathbf{m_{(PR)}}$, the total amount of carbon present in a batch of PR wafers $\mathbf{m_{C\ (PR)}}$ can was determined following the equations (2) and (3):

$$\mathbf{m_{C\ (PR)}} = \mathbf{m_{C\ (Resin)}} + \mathbf{m_{C\ (PAC)}} \qquad (2)$$

$$\mathbf{m_{C(resin)}} = ((\mathbf{m_{(PR)}} \,.\, \mathbf{fr_{(resin)}}) / \mathbf{M_r(FU)}) \,.\, \mathbf{x} \,.\, \mathbf{12{,}0} \qquad (3)$$

The total amount carbon in the PR can be considered as the sum of the carbon present in the resin structure of the PR and the amount of carbon present in the Photo-Active Compound (PAC). The amount carbon in the solvent, ethyllactate for the I-line resist and a mixture of ethyllactate and PGMEA for the DUV resist, was not considered in first instance because only a very small amount of solvent remains after the spinning procedure.

The total mass of carbon present in the resin of the PR ($\mathbf{m_{C(resin)}}$ in g) can be calculated from the number of moles functional units in the resin (calculated by multiplying $\mathbf{m_{(PR)}}$ with the fraction of resin $\mathbf{fr_{(resin)}}$ present in the PR and dividing by the molar mass of one functional unit ($\mathbf{M_r(FU)}$). Once the number of moles is known, one has to multiply by the number of carbon atoms in one functional unit (**x**) and the atomic mass of carbon (**12,0** g/mole). The calculation for the PAC is similar.

For I-line resist, one functional unit in the resin contains 8 carbon atoms and the molar mass M_r was 120 g/mole corresponding to the structure of the Novolak resin[15,16,17,18]. Typical mixing ratios lay in the range of 75 % to 85 % resin, leaving 25 % to 15 % PAC. One functional PAC unit (diazonaphtoquinone structure) had a molar mass of 284.6 g/mole and contains 10 carbon atoms. For DUV resists only small amounts of PAC were present, typically ranging between 95 and 99 %. Following parameter values were used in the calculations: FU(Resin): 13 carbon atoms, M_r = 220.0 g/mole and FU(PAC): 14 carbon atoms, M_r = 354.5 g/mole.

The results for the calculations for the I-line resist are given in Table 1. In this table [C] is the total concentration of carbon in ppm present in the reclaim tank, $\%C_{TOC}$ is the fraction of photoresist carbon converted to TOC in the process water, $\%C_{TIC}$ is the fraction converted to TIC in the process water and $\%\ C_{GAS}$ is the remaining fraction PR carbon which can be assumed to be converted to CO_2 and volatile organic carbons.

Table 1: Distribution of the I-line photoresist carbon in the various fractions TOC, TIC and in the gas phase

ρ (g/cm³)	% Resin	% PAC	[C] (ppm)	% C_{TOC}	%C_{TIC}	% C_{GAS}
1.00	85	15	50.15	70.08	7.12	22.80
	75	25	47.60	73.84	7.50	18.66
1.20	85	15	60.18	58.40	5.93	35.67
	75	25	57.12	61.54	6.25	32.21

From this table it is clear that the largest fraction of the carbon present in the PR ends up in the process water under form of organic compounds. Also a considerable amount of the carbon is converted to gaseous compounds. For the DUV resist similar results were obtained.

Chromatographic Analysis The I.C. chromatogram of the I-Line sample is shown in Figure 2. The major compounds were acetic acid, formic acid and oxalic acid while glyoxilic acid and pyruvic acid are of minor importance and ketomalonic acid is near the detection limit.

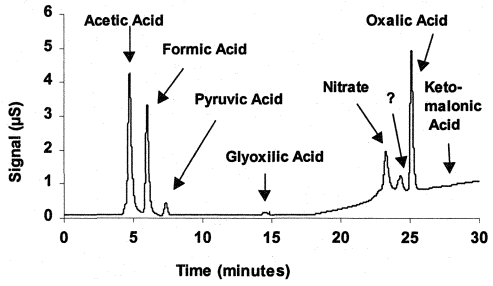

Figure 2: I.C. Chromatogram of the I-line sample

For the DUV sample similar results were obtained, except for the absence of pyruvic and ketomalonic acid.

In both the I-line and DUV samples, a large variety of compounds were identified with Dynamic Headspace GC-MS. All these compounds were present in very low concentrations (below 100 ppb) and almost the same compounds were seen for the two types of PR as is shown in Table 2.

Table 2: Identified compounds with Headspace GC-MS

Aldehydes	**Ketones**	**Alcohols**	**Carb. Esters**
Formaldehyde	Di acetyl	Ethanol	Me-Formiate
Acetaldehyde	2-Butanone	t-Butanol	*Et-Formiate*
Propanal	2-Pentanone		Me-Acetate
Butanal			**Et-Acetate**
2-Propenal			
2-Me-Propanal			
2-Me-2-Propenal			

The compounds printed in Italic, Propanal and Et-Formiate, were only identified in the I-line sample while the compounds printed in bold were only determined in the DUV sample.

Carbon balance On the basis of a quantitative analysis, the total amount of carbon present in these compounds was calculated. In combination with the TOC measurements, a carbon balance was made. It is clear that carboxylic acids are the most important

degradation products of PR after O_3 processing. The compounds identified with HS GC-MS only form a minor fraction.(Table 3)

	% Carb. Ac.	% HS GC-MS	% Missing
I-Line	42.56	0.38	57.06
DUV	25.84	1.47	72.69

Table 3: Distribution of the categories of identified compounds related to the total amount of PR carbon

From these data it is also clear that the largest fraction of the organic carbon present in the process water could not be identified yet. Possible reasons for the large gap in the carbon balance could be the presence of compounds with a number of carbon atoms higher than 5, which would mean that not all PR is converted to small fragments with a number of C-atoms lower then 5. Another possibility is that some compounds show a very poor sensitivity with the Headspace GC-MS detection techniques. In general, compounds with high Henry Coefficients tend to remain in the solution and are not easily outgassed. As such detection with HS GC-MS is not a suitable technique for this type of compounds. Characteristic examples are glyoxal, formaldehyde and methanol.

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METALS

ENGINEERING TOOLS FOR DESIGNING A METALLIC REMOVAL SOLUTION

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In this paper, an overview and an analysis is given of the different engineering tools that are at our disposal for designing a metallic removal solution

INTRODUCTION

Wet chemistry is the most powerful and the most versatile process available today to remove metallic impurities from surfaces. The state of the elements in the solution is the first important aspect of any wet cleaning chemistry. There are quite a few engineering tools available to predict any contaminants' state in any kind of solution. The next important aspect is the state of the surfaces on wafers. Almost all surfaces of interest can be divided in 2 main groups: the hydroxide terminated oxide or the hydride terminated silicon surface. Both surfaces react very differently with metallic impurities and therefore, the adhesion mechanisms, the adsorption forces and the cleaning solutions should be understood. Different engineering tools exist to approach these questions.

ENGINEERING TOOLS

The important parameters for cleaning metallic impurities from surfaces are:
- State of the elements in the solution
- State of the surface to be cleaned
- Interactions between the surface and metallic ions

All of the interactions can be understood and modeled by using the following engineering tools:
- Pourbaix diagram
- Standard Reduction Potential Table
- Solubility Product Table
- Reaction constants with silica gel
- Analogy with hydrolysis behavior
- Hydrolysis prediction

- Hydroxides solubility contstants
- Evans diagram
- Chelating agent constants

It is important to understand the usefulness and the information provided by each different engineering tool.
The first engineering tool is the Pourbaix diagram. An example of the Pourbaix diagram for Cu is shown in fig. 1.

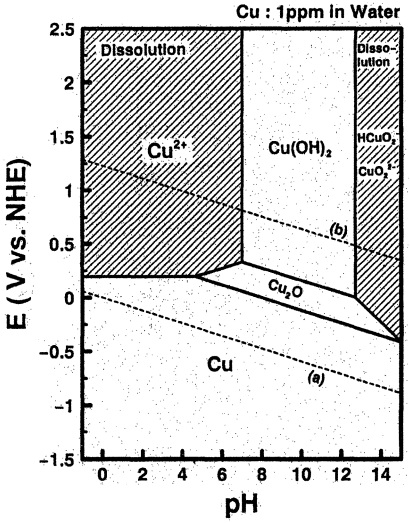

Fig. 1. Pourbaix diagram for Cu.

The Pourbaix diagram is useful in many ways. E.g. in order to review the state of the elements or impurities in solution. The Pourbaix diagram represents the State of the elements a.f.o. pH, redox potential, interacting anions. One has to remark however that it is important to review the interactions that are taken into account when constructing the diagram. The second engineering tool is the standard reduction potential table. This is shown in table 1.
The disadvantage of this table is that it only provides a 1-dimensional cut of the Pourbaix diagram. The advantage is that more reactions/interactions can be taken into account than in the Pourbaix diagram.

Table 1. Standard reduction potential table.

	E^0 (V vs. NHE)
$O_3 + 2H^+ + 2e^- \Leftrightarrow O_2 + H_2O$	2.07
$H_2O_2 + 2\,H^+ + 2e^- \Leftrightarrow 2H_2O$	1.776
$Au^{3+} + 3e^- \Leftrightarrow Au$	1.50
$O_2 + 4H^+ + 4e^- \Leftrightarrow 2H_2O$	1.229
$Ag^+ + e^- \Leftrightarrow Ag$	0.799
$Cu^+ + e^- \Leftrightarrow Cu$	0.521
$Cu^{2+} + e^- \Leftrightarrow Cu$	0.337
$2H^+ + 2e^- \Leftrightarrow H_2$	0.000
$Pb^{2+} + 2e^- \Leftrightarrow Pb$	-0.126
$Ni^{2+} + 2e^- \Leftrightarrow Ni$	-0.257
$Fe^{2+} + 2e^- \Leftrightarrow Fe$	-0.440
$SiO_2 + 4H^+ + 4e^- \Leftrightarrow Si + 2H_2O$	-0.857
$A^{3+} + 3e^- \Leftrightarrow Al$	-1.662
$Mg^{2+} + 2e^- \Leftrightarrow Mg$	-2.37
$Na^+ + e^- \Leftrightarrow Na$	-2.714

The 3rd engineering tool is the solubility product table shown in table 2 for the hydroxides.

Table 2. Solubility product table for the hydroxides.

Solubility of selected metal hydroxides at pH=7 and pH=10

Metal	*Solubility (ppb) at pH=7*	*Solubility (ppb) at pH=10*
Al^{+++}	$5*10^{-4}$	$5*10^{-13}$
Ca^{++}	Very high	Very high
Cu^{++}	$1*10^{3}$	$1*10^{-3}$
Co^{++}	$6*10^{6}$	6
Fe^{++}	$2*10^{5}$	0.2
Fe^{+++}	$1*10^{-10}$	$1*10^{-19}$
Pb^{++}	300	$3*10^{-4}$
Mg^{++}	Very high	$1*10^{4}$
Mn^{++}	Very high	$1*10^{3}$
Hg^{++}	$6*10^{-4}$	$6*10^{-10}$
Ni^{++}	$3*10^{6}$	3
Sn^{++}	$6*10^{-5}$	$6*10^{-11}$
Zn^{++}	$4*10^{5}$	0.4

The solubility product table of the hydroxides can be used to read out the hydrolysis tendency and therefore the reaction of metallic ions with the silanol groups on the wafer surface. It also shows the precipitation behaviour of metal hydroxides.

Tool nr. 4 are the literature values for silica gel. These constants provide a numerical value to calculate the coverage of the SiO_2 surface with metallic ions.
Tool nr. 5 are the hydrolysis constants. Reaction constants of metallic ions with the silanol surface can be derived from its hydrolysis constant, which can be found in the literature.
Tool nr. 6 is the hydrolysis constant prediction. If the hydrolysis constants are not available or not easily looked up, one can use the charge number and the ionic radius to predict a metals hydrolysis constant.
The hydrolysis constant can also be predicted by using engineering tool nr. 7, which provides us with a prediction based on the hydroxide precipitation table or alternatively the Pourbaix diagram.
The 8th tool available to a cleaning engineer is the Evans diagram. The Evans diagram can be used to calculate the potential of the surface and is important when dealing with bare silicon surfaces. An example of the Evans diagram is shown in fig. 2.

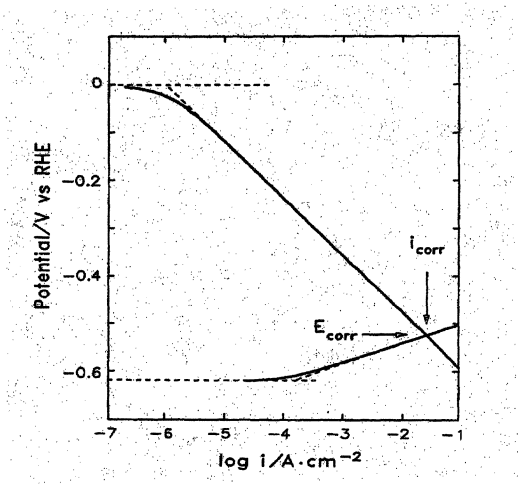

Fig. 2. Evans diagram for Fe in H_2O.

The last tool available is the chelating agent constant tables. These should be used when engineering cleaning solutions with chelating agents.

SUMMARY

In this paper the different engineering tools for approaching metallic impurity interactions with the wafer surface are presented. A thorough understanding of all these tools is fundamental for any cleaning engineer.

REDUCTION OF SURFACE METALLIC CONTAMINATION THROUGH OPTIMIZED RINSING AND SINGLE-WAFER DRYING

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The increasing trend towards clustering of processing tools calls for fast and efficient rinsing and drying techniques for single wafer processing. Classical single wafer spin dryers still leave a film of several micron to evaporate. All non-volatile contaminants still left in this film will re-deposit on the wafer surface. It is therefore crucial to minimize the amount of evaporated liquid during the drying step. A novel drying technique (Rotagoni^{TM}) that can be used at low rotational speeds was recently proposed. Tests with concentrated KCl solutions showed that after Rotagoni drying the evaporated film thickness is at least two decades lower when compared to classical spin drying. Tests with Ni salt in lower concentrations indicated that adsorption of metallic contamination during the rinse step prior to drying can become dominant. Very low levels of surface metallic contamination can be obtained by combining the Rotagoni drying technique with an acidified rinsing step.

INTRODUCTION

In semiconductor device fabrication, it is crucial to keep surface metal and particle concentrations extremely low to ensure optimum yield [1]. This is usually accomplished by a sequence of wet cleaning, rinsing and drying steps. The rinsing step is nothing else than a dilution of residues left behind after the last cleaning step. Therefore very long times are required to allow for transport of these residues into the bulk of the rinsing liquid [1,2]. For finite rinsing times a residual fraction of contaminants can remain in a liquid film close to the wafer surface. Upon evaporation of this film in the drying step these contaminants will redeposit on the wafer surface. It is therefore crucial that rinsing and drying procedures are optimised in order to minimize the residual amount of surface contamination.

In batch type systems, wafers are often dried in a spin dryer [1, 3]. However, the spin drying process is very sensitive to what is commonly denoted by the term "drying marks", "stains" or "streaks". These drying marks are believed to be residues (from suspended particulate matter, dissolved silica or salts) that deposit when liquid droplets evaporate from the surface [3–7]. For more critical process steps, IPA vapour dryers were introduced. They showed a significant improvement in particle performance when compared to the spin dryers. However, IPA consumption and safety

issues (boiling IPA) were a major drawback [1, 3]. Current state-of-the-art tools also use some soluble surface tension reducing agent (often still IPA) but in considerably less amounts [3].

Recent trends in industry predict more and more clustering of cleaning tools with production equipment. This calls for faster and more efficient single wafer cleaning equipment. For single wafer drying, however, one still uses in most cases a high speed spinning process. Since very few alternatives are available to overcome the problems associated with spin drying, we recently proposed the Rotagoni^{TM}drying technique [8]. It has the advantage of being able to operate at low rotational speeds. This can significantly reduce the amount of splash back and entrainment of airborne particulates [9] when compared to spin drying. Further details on the process can be found elsewhere [8, 10–12]. In this paper we will use spin drying as a benchmark to evaluate the performance of the Rotagoni^{TM}drying technique. The figure of merit is the amount of liquid that is evaporated from the wafer surface after the drying step. This will be done both theoretically and experimentally using tests with concentrated KCl solutions. Metallic contamination, however, can also occur during the final rinse step. Therefore the effect of pH during the rinse and the interaction with the drying technique applied will be investigated as well. This is done using tests with dilute nickel solutions.

PROCEDURE

Model

The amount of surface metallic concentration C_{surf} present after a final rinse and drying step can be written as

$$C_{\text{surf}} = h_{\text{film}} C_{\text{liquid}} + C_{\text{adsorption}} \tag{1}$$

where h_{film} represents the thickness of the film that evaporates during the drying step, C_{liquid} is the metallic concentration in the rinsing liquid and $C_{\text{adsorption}}$ represents the amount of adsorbed metallic contamination. The first term in the right hand side of equation (1) is due to the drying process, while the second term can be attributed to the rinsing step.

When a high concentration of ions is present in the liquid, the first term is dominant and we can write equation (1) as

$$h_{\text{film}} = \frac{C_{\text{surf}}}{C_{\text{liquid}}} \tag{2}$$

Using this equation we can calculate the thickness of the liquid film that evaporates provided that C_{liquid} and C_{surf} are known. This was done in this work for spin drying and Rotagoni drying using a 1000 ppm KCl solution.

For low concentration of ions, such as e.g. during a rinse step with UPW, the second term in equation (1) can be the dominant term. This was investigated in this work by using dilute Ni solutions.

Experimental

All tests were performed on 200 mm <100> p-type Cz silicon wafers obtained from Wacker Siltronic. Wafers were precleaned using an Imec clean [13] in a Steag-Mattson automated wetbench. This clean consists of a sequential treatment in H_2SO_4/H_2O_2 and dilute HF, followed by a dilute HCl/O_3 rinse and an acidified Marangoni dry step. The ozone added to the final rinse renders the Si wafer surface hydrophilic.

KCl solutions were prepared from high purity (> 99.9%) KCl salt (Aldrich) in UltraPure Water (UPW) water. Ni solutions were prepared from 1000 ppm standard solutions in 0.5M HNO_3 (Merck). The pH was adjusted by adding ppb grade HCl (37 w%, Ashland) and measured using a double junction sleeve glass electrode with a model 477 pH meter from Metrohm.

Spin dry and Rotagoni tests were performed on two platforms. The first platform was based on a bench top wafer spinner onto which a moveable arm was mounted. Two dispense tubes mounted on this arm deliver IsoPropylAlcohol (IPA) vapour and UPW water respectively. The IPA vapour was generated by bubbling N_2 gas through a bubbler filled with liquid IPA at room temperature. In line measurements with an IR sensor (IRS 2000 NDIR analyzer, ORB analytical company) indicated that the IPA weight concentration was approximately 5%. UPW flow was in the order of 100 ml/min. It should be noted that for the salt tests the UPW was replaced with the same salt solution as for the spin dry tests. Delivery of the salt solution to the nozzle was done using a N_2-pressurized canister. The second system consisted of a Verteq Goldfinger^{TM}platform onto which also a moveable arm was mounted. Dispense of IPA vapour and liquid was done in a similar way as on the first system.

Analysis of surface metals was done using an Atomika XSA 8010 Total Reflection X-Ray Fluorescence spectroscopy tool (TXRF). The operating settings were 50 kV at 50 mA using the $K\alpha$-line of a Mo tube for excitation. The incident angle of the X-rays was 1.3 mrad and the total measurement time was 1000 seconds per point.

RESULTS AND DISCUSSION

Theoretical considerations on drying

Spin drying The starting point for calculations of a residual liquid film is the well-known Landau-Levich equation [14]. This equation gives the thickness h of a liquid film entrained by a solid that is withdrawn from a solution as

$$h = 0.946\sqrt{\frac{\sigma}{\rho g}}Ca^{2/3} \tag{3}$$

Where $Ca = \eta\, v/\sigma$ is the capillary number and σ, ρ and η denote the liquid surface tension, density and dynamic viscosity, respectively. The term g is the gravitational constant and v denotes the speed of withdrawal. (Note that this equation strictly is only valid for low values of the capillary number). Applying equation (3) to typical process conditions one finds that the resulting film thickness when wafers are taken from a bath of water (or likewise in a quick dump tank, where the liquid is drained from the bottom) is in the order of 20 μm [1, 2]. This thickness can be significantly decreased by spinning the wafers at high speed. Models describing the flow of a liquid film on a rotating substrate are readily available in the literature and are usually concerned with the photoresist spin coating process. The earliest of such analysis is due to Emslie et. al. [15]. This model gives the film thickness of a non-volatile newtonian liquid on an infinite rotating disk:

$$h(t) = \frac{h_0}{\sqrt{1 + \frac{4\rho\omega^2 h_0^2 t}{3\eta}}} \tag{4}$$

where h_0 is the initial film thickness and ω is the wafer rotation speed. Equation (4) shows that the final film thickness goes to zero for infinite spinning times. However, since this model does not take evaporation into account, this behaviour is only true for liquids with extremely low vapour pressure. In practical cases (and also for the case of spin drying of water films) evaporation should definitely be taken into account. Meyerhofer [16] extended Emslie's model to include the effect of evaporation on film thinning. In his calculations he found that the spinning process can actually be divided in two subsequent phases: (i) a first phase where convective outflow dominates and (ii) a second phase where evaporation takes over. As a result of this, Meyerhofer was able to derive an equation for the dependence of final film thickness on spin speed ω, initial viscosity η and evaporation rate e:

$$\lim_{t\to\infty} h(t) \propto \omega^{-2/3}\eta^{1/3}e^{1/3} \tag{5}$$

Assuming that evaporation e is proportional to the air flow over the disk (derived by Cochran [17] as being proportional to $\sqrt{\omega}$) one then obtains:

$$h_{film} = \frac{a}{\sqrt{\omega}} \tag{6}$$

where h_{film} is the evaporated film thickness, i.e. $h_{\text{film}} = \lim_{t\to\infty} h(t)$. This equation is in agreement with empirical data of various other researchers [18–21]. Equation 6 indicates that the final film thickness only depends on the wafer spinning speed and no longer on initial film thickness, as was the case with equation (4).

Rotagoni drying The mechanism of the Rotagoni drying process is believed to be a manifestation of interfacial turbulence [22] due to a surface tension gradient (also

commonly denoted as the *Marangoni-effect*). A qualitative description can be found in the literature on Marangoni drying of silicon wafers. In their pioneering work in 1990, Leenaars et. al. [23] already explained the effect of a soluble tensioactive vapour on the drying process. When a meniscus exists at a solid substrate immersed in liquid, the tensioactive vapour that starts dissolving in the liquid will diffuse away to the bulk. In the thin part of the meniscus, however, the concentration of tensioactive compound will increase very fast compared to the bulk liquid away from the meniscus. This results in a surface tension gradient that causes a convective liquid flow from the thin part of the meniscus toward the bulk of the liquid. Experimental values on the remaining film thickness after vertical withdrawal from a $CoCl_2$ solution were obtained by Marra and Huethorst [24]. For 2-propanol they measured thicknesses between 14 and 160 nm, depending on experimental conditions. A mathematical model describing Marangoni drying was also recently developed [25]. In this model a fixed surface tension gradient τ was imposed as a boundary condition. The entrained film thickness is then found to decrease monotonically from the Landau-Levich result (see equation (3)) to zero, as function of τ. Since a comparison of this model with experimental data [24] indicate that the Marangoni force is by far dominant over viscous forces it is our belief that as a first approximation it can also qualitatively describe the Rotagoni process. We therefore expect the final film thickness after Rotagoni drying to be of the same order of magnitude as obtained by Marra and Huethorst [24].

Experimental verification

Spin drying The film thickness during spin drying was experimentally determined based on equation (2). A solution containing 1000 ppm KCl was dispensed for 5 seconds on a wafer and spun at 500 rpm for a certain time after which the spinner was stopped. The remaining film was left to evaporate in the ambient air and the surface concentration of K and Cl was analysed by TXRF on 12 points per wafer.

These measurement points were equally spaced at 90 degree angles on concentric circles of different radii. No significant influence of radius was observed and the resulting error bar calculated for all measurement points is below the marker size. The horizontal error due to spinner acceleration and deceleration is taken as 3 seconds. The result of two independent tests is given in figure 1, together with some fits following equation (4) for various values of h_0. The experimental points in figure 1 show a rapid decrease in film thickness in the first 20 seconds, after which the thickness remains more or less constant. It is clear that the model without evaporation is inadequate to describe this data. A full description of the spin drying process would require various modifications of this model [16,26,27]. Since we are mainly interested in the resulting film thickness after the drying process is complete, the validity of equation (6) was verified experimentally. A 1000 ppm KCl solution was dispensed for 5 seconds and wafers were spun at different rotation speeds until visually dry (see figure 2). Each marker represents the average of four equally spaced measurement

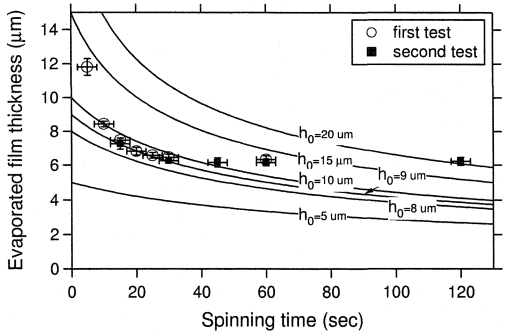

Figure 1: Evaporated thickness (based on K-signal from TXRF) for 2 tests at 500 rpm. Solid lines represent model from equation (4) for different values of h_0.

points on a circle of radius 50 mm. Error bars are comparable to the marker size. One can see that the experimental data can be well fitted by equation (6) where $a = 127.8[\mu m\sqrt{\text{rpm}}]$ with a standard deviation of 2.5. This equation allows us to predict the evaporated thickness for a given spinning speed.

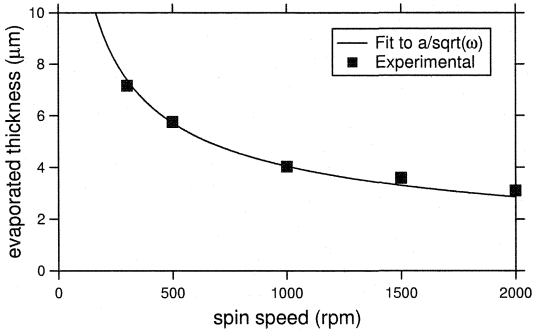

Figure 2: Final film thickness after spindrying

Rotagoni drying To estimate the evaporated film tickness for the Rotagoni process a similar test with a 1000 ppm KCl solution was performed. A wafer was prewetted with KCl solution and dried with the Rotagoni process. It should be noted that during the drying step the liquid dispensed was spiked with the same concentration of KCl. This avoids any dilution effects. A comparison between Rotagoni and spin drying is made in figure 3. In this figure, each marker represents a TXRF measurement.

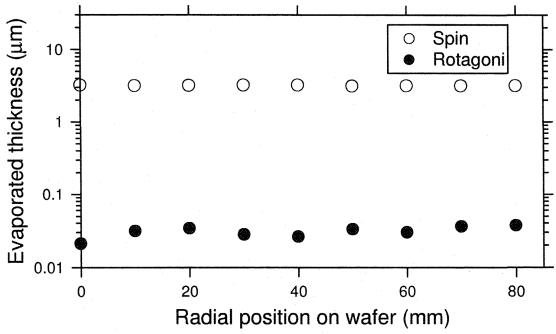

Figure 3: Evaporated thickness values (based on K signal) for spin dry at 1800 rpm and rotagoni at 300 rpm (nozzle speed=1mm/s).

We can estimate the thickness after Rotagoni dry to be between 20 and 50 nm, which is about two decades lower than spin drying. This value is in very good agreement with the results obtained by Marra and Huethorst [24] who found 14 nm when a directed IPA vapour was used at a withdrawal speed comparable to the Rotagoni nozzle speed.

Adsorption

Low metal concentration In all preceding tests described in this paper, a highly concentrated KCl solution was used (> 100 ppm). In that case one can safely use equation (2) to calculate the film thickness. For very dilute solutions, the resulting surface coverage becomes very low and metal adsorption can be the dominant mechanism [28]. This was evidenced by repeating the experiments with Ni solutions in a lower concentration range (100ppb – 100ppm). The solutions were prepared by diluting a standard solution of 1000 ppm Ni^+ + 0.5M HNO_3 with UPW. It was found that the calculated thickness values from the Ni data using equation (2) were systematically overestimated when compared to the KCl tests. This deviation became more and more pronounced for lower Ni concentrations. The reason is that with decreasing Ni concentration the first term in equation (1) decreases and the adsorption term becomes more and more important. In this case equation (2) can no longer be used. Instead of the calculated film thickness, we therefore plot the measured surface concentration vs the concentration of Ni in solution (see figure 4).

The dashed lines represent the predicted amount of Ni due to evaporation for typical film thickness values obtained for spin drying ($h_{film} \simeq 3\mu m$) and for Rotagoni^{TM}drying ($h_{film} \simeq 50nm$) as can be taken from figure 3. For high Ni concentrations in the liquid we can see again the two decade difference between both drying techniques. At this point the experimental points coincide with the dashed

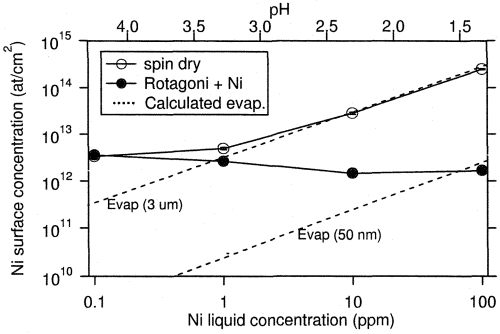

Figure 4: Surface concentration of Ni vs amount of Ni in liquid phase. The dashed lines represent calculated Ni concentrations for evaporated film thickness of 3 μm and 50 nm (see also figure 3.

lines, indicating that the measured surface contamination is primarily due to evaporation. For the conditions with less Ni in solution the experimental data deviate more and more from these curves and for the lowest concentration tested the amount of adsorbed metals completely dominates for both spin dry and Rotagoni dry. It should be noted that because the Ni solutions were prepared by dilution with UPW the pH of each dilution was different. This is plotted on the top axis. Therefore one can not distinguish whether the observed phenomenon has to be attributed to the Ni concentration, the solution pH, or both.

Effect of pH The adsorption of cations on hydrophilic Si wafers has already been studied by other researchers [28–31]. They assumed that the Si-OH groups at the SiO_2-surface act as weakly acidic ion-exchange sites with the cations from solution. The equilibria governing this process can be written as:

$$\equiv \mathrm{SiO^-(s)} + \mathrm{H^+(aq)} \overset{K_\mathrm{H}}{\rightleftharpoons} \mathrm{SiOH(s)} \tag{7}$$

$$\equiv \mathrm{SiO^-(s)} + M^{n+}\mathrm{(aq)} \overset{K_M}{\rightleftharpoons} \mathrm{SiO}M^{(n-1)+}\mathrm{(s)} \tag{8}$$

where K_H and K_M are the reaction constants that describe the adsorption of H^+ and M^{n+} onto the surface, respectively. Furthermore it is assumed that there is a finite concentration, σ_0, of common available adsorption sites on the surface and that cations (M^{n+} but also H^+) attach singly to these surface sites. In case only one cation is present in addition to H^+ we can write the following surface concentration balance:

$$\sigma_0 = \sigma_{\mathrm{SiO}M} + \sigma_{\mathrm{SiOH}} + \sigma_{\mathrm{SiO^-}} \tag{9}$$

where σ_{SiOM} is the surface concentration of the metal on the wafer surface. Combining equations (7), (8) and (9) one obtains the following expression for the metal surface concentration:

$$\sigma_{SiOM} = \frac{K_M[M^+]}{1 + K_H[H^+] + K_M[M^+]}\,\sigma_0 \tag{10}$$

Equation (10) is equivalent to the Langmuir model for gas adsorption [32]. It shows that the H^+-ions are competing with the metal ions in the solution. Increasing the relative amount of H^+ vs M^+ – by lowering the pH – will decrease the amount of M^+ on the oxide surface. Solutions containing 100 ppb of Ni with various pH-values were used to compare spin dry with Rotagoni (see figure 5). It can be seen that lowering the pH results in a decreased amount of metals on the wafer surface. For the higher

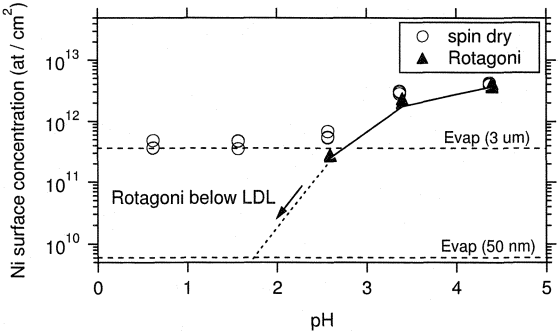

Figure 5: 100 ppb Ni rinsing test at low pH. Each marker represents a TXRF measurement point. One wafer was used per condition.

pH values both curves coincide since the adsorption of Ni at the oxide surface is the dominant mechanism. This corresponds well with the data from figure 4 where both curves also coincide at low Ni concentrations. At low pH (< 3) the measured surface concentration is below the lower detection limit ($\simeq 10^{11}$at/cm^2) for Rotagoni drying while for spin drying the surface concentration remains constant. This is because deposition from the evaporated layer is now dominant. These results clearly indicate that a combination between acidified rinsing and Rotagoni drying can drastically reduce surface metallic contamination.

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CONCLUSIONS

The amount of surface metallic contamination present after a wet cleaning step is given by the adsorption during the rinsing step and the deposition from the evaporated liquid film during the drying step. The latter can be reduced by using a drying technique that minimizes the evaporated film thickness. Test with a tracer solution indicate that spin drying leaves residues from a film of several micron thick, while after the Rotagoni^{TM}a film of only a few tens of nanometer thick evaporates. This is an improvement by approximately two decades. This also significantly reduces the risk of drying marks since less water containing dissolved silica is left to evaporate from the wafer. The adsorption of metallic species can be reduced by lowering the *pH* of the rinsing step. It was found that the combination of acidified rinsing with Rotagoni drying can significantly decrease the residual amount of surface metallic contaminants after a wet cleaning step.

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DIFFERENT ADSORPTION BEHAVIORS OF PLATINUM GROUP METALS ON SILICON SURFACES

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We have investigated the adsorption behaviors and the removal efficiency of platinum group metals on single crystalline silicon surfaces. The impurities contaminated on the surfaces are hardly removed even by the acidic solutions with high oxidation-reduction potential values. Moreover, a number of large-sized metallic induced pits are observed on the entire surface after cleaning of hydrofluoric acid containing solution. When the various noble metals are contaminated on the surfaces, the contamination levels of metals such as Cu, Ag, and Au are proportional to the contaminants concentration on the surfaces, while the deposited amount of Pt group metals (Pt, Ir, Ru) is very low. However, the Pt contamination level in NH_4OH solution with high pH value is two orders magnitude higher than other impurities (Ir and Ru). The pH value control in the chemical containing solutions is mandatory to avoid Pt contamination onto the substrate surface. These results lead to the conclusion that wet cleaning methods cannot remove Pt group metallic impurities from the silicon; the amount of adsorbed metallic impurities on the surfaces can be minimized by optimum selection of cleaning solutions.

INTRODUCTION

With process of semiconductor industry, new device is becoming more integrated and cell structure is becoming more complicated, so that, this brings in many difficult challenges [1]. The basic requirements for future gigascale integration (GSI) devices are the reduction of minimum feature size with device integration and high-speed operation

with sufficient cell capacitance. Many films comprising electrodes and dielectric materials should be altered to meet device requirements. Moreover, as the allowance level of contaminants on substrate surfaces becomes more stringent, the cleaning importance for removing them becomes even more important. This is because the semiconductor process for high quality device fabrication will never be realized without perfect cleaning on all surfaces. When the conventional cleanings are applied to the exposed surfaces of various metal films, they caused serious problems such as rapid etching rate of metal films and pattern lifted off from the surface [2], [3]. Therefore, we pointed out that the target of wet cleaning should be beginning the transition from GSI device fabrication employing various new metals and dielectric films to avoid the serious problems. That is, future wet cleaning is required to aim for not only lowering cost of ownership (CoO) and promoting Environment, Safety and Health (ESH), but improving cleaning performance on metal film exposed surfaces or tiny patterned surface structure [4] ~ [6]. In addition, we should pay attention to the control of the newly introduced noble metals such as Cu, Pt, Ir, Ru, and etc [1]. It is reported that the metal impurities with an electronegativity higher than the silicon (Si) take electrons from the surface, and hence forming direct chemical bonds with surface [7]. They are easily contaminated onto the surfaces and their removal is very difficult using various cleaning solutions.

The platinum group metals are strong candidates for electrode films of high dielectric films in the future, but the adsorption behaviours and the removal efficiency are not clear yet. The present work focuses on a method to avoid the Pt group metal contamination on the substrate surfaces in great detail.

EXPERIMENTAL

Two types of crystalline silicon (c-Si) wafers used were type A [8-in. p-type (100) oriented wafers with resistivity of 10 Ω·cm] and type B [8-in. n-type (100) oriented wafers with 3 to 5 Ω·cm]. The samples are pre-cleaned by a sequential cleaning of sulfuric acid-hydrogen peroxide mixture (SPM: 4:1, 90°C) for 10 min., a 0.5% HF for 30 sec., and post ultrapure water (UPW) rinse with a resistivity of 18.2 MΩ·cm for 10 min. In order to investigate the relationship between the amount of adsorbed metals and metal impurity concentration in wet bath, the wafers are contaminated using various contaminants, and hence dried by a blowing using an ultrapure nitrogen gas. Following, these contaminated wafer surfaces were cleaned in various chemical solutions. In every cleaning process, the cleaning time was set to 10 min followed by a UPW final rinse for 10 min., and dried with ultrapure nitrogen gas.

The amount of deposited metallic impurity is analyzed with an incident angle of 0.05 degree by Total Reflection X-ray Fluorescence Spectroscopy (TRXRF) system using W x-ray source of 30 kV and 200 mV and Mo x-ray source of 40 kV and 40 mV. The source selection of W or Mo depends on the kinds of metal impurities.

RESULTS AND DISCUSSION

Figure 1 compares the dependence of metals removal efficiency on various chemicals with high oxidation-reduction potential (ORP) value. It is well known that the removal of noble metal impurities from silicon substrate is very difficult [8]. The platinum (Pt) impurities on silicon surface are intentionally contaminated by use of spinner system using Pt.HCl (1mol/l) solution. In other words, the others were deposited by dipping into UPW spiked with different metal contaminants such as $CuCl_2$, Ag_2SO_4, and Au (in 10% HCl solution). This is due to the fact that the Pt impurities on the surface are not deposited by conventional dipping method with comparing to the case of the other metals. The cleaning methods with high ORP value have a good efficiency to remove metallic impurities such as Cu and Ag, but the amount of Pt and Au residues does not change so much. The different removal rates from the contaminated surfaces by various solutions can be attributed to the difference of electronegative value with the species of noble metals. Figure 2 is typical SEM pictures of Pt contaminated c-Si surfaces for 10 min *before and after* FPM (HF/H_2O_2 = 0.5 w-%/0.5 w-%, RT) cleaning. We point out that the number of Pt particles on the surface after the cleaning are not decreased so much. Moreover, a number of large-sized metallic induced pits (MIPs) are observed on the entire Si surface after the cleaning, which well agrees with the contamination level measured using a TRXRF system (fig.1). In order to prevent the impurity contaminated substrates from formatting them, much more attention should be given for wet cleaning process.

Figure 3-a and –b represents the etching rates of metal films as a function of increasing HF concentration in dilute HF (dHF) only and H_2O_2 concentration in FPM, respectively. The data are calculated from the sheet resistance measurement using the four points probe technique and -when indicated- the results can be extended to other materials. When the concentration in dHF being increased (fig. 3-a), the etch rates of light metals (Co, Al and Ti) and silicide films (WSi_2, $CoSi_2$ and $TiSi_2$) of 13 metal samples are increased. In other words, the others (Cu, TiN, W, and WN) including platinum group metals (Pt, Ir, and Ru) have low etching rate less than 0.1 nm/min. In case of Cu film, even though ionic state is stable at high HF concentration range, the rate is very low to be ignored. Both W and WN films are not etched at all because they exist in surface immunity or passivated state in the solution, not ionic state. However, the rates of the metals except Pt groups also increase with the increase of H_2O_2 concentration in a 0.1% HF solution (fig. 3- b). It is important to note that adding oxidant even at constant HF concentration can control the etching rates of metallic films. The H_2O_2 addition in HF solution leads to increasing ORP value without changing pH value, so that, it supplies driving force to promote ionization of metallic films. In other words, platinum group metals such as Pt, Ir, and Ru act as a catalysis of H_2O_2 decomposition, which is directly dissolved without proceeding etching reaction from their surfaces. The metals are not etched in solutions even with very high ORP and low pH values such as SPM and SC-2 ($HCl-H_2O_2-H_2O$ with a mixing ratio 1:1:6 at 85°C) solutions [2]. We observed a large number of bubbles generation from the Pt film surface in H_2O_2 containing HF solution instead. The required electrons for oxidant decompositions in solution are not generated from the metal surfaces; rather, the decomposition of H_2O molecules can give the electrons to the surface, due to high elctronegativity value of the

metallic Pt group. Judging from the results between the removal efficiency (fig.1) and the etching rate (fig.3), a lager number of the Pt particles after FPM cleaning were found on the surfaces (fig.2) –as expected– since the solution doesn't have dissolution capability for the particles from the substrate [3]. A new chemical that has a function to dissolve the impurities onto the surfaces should be studied for removing them from substrates. In order to avoid the contamination onto the surfaces, it is therefore mandatory to perfectly separate the wafers from the contaminants during process.

Figure 4 represents the adsorption characteristics of noble metal impurities including Pt group metals. The hydrophobic silicon surface that is characterized by hydrogen termination [9] is contaminated by dipping into UPW spiked with different metallic contaminants. The contamination level of the metals such as Cu, Ag, and Au is proportional to the contaminants concentration, while the deposited amount of Pt group metals is very low. That is, the Pt group impurities in wet solutions appear to be not deposited on the c-Si surfaces. We point out that the amount of deposition of the Pt group metals is smaller than that of Cu, even though their electronegative values are higher than that of Cu.

Figure 5 shows the dependence of 3 metals adsorption behaviours on adding 1 ppm contaminants to various chemicals, where the concentration of the added chemicals in this study is fixed at 1 mol/l. The amount of adsorption after 3 min is not so high regardless of added acidic solutions. However, the amount of Pt impurity in NH_4OH solution is uniquely increased by 2 orders of magnitude larger than those in acidic solutions. From the result, it is recognized that the adsorption behavior of Pt contaminants is different from those of Ru and Ir impurities. The tight pH value control in wet cleaning solution seems to be very important to avoid Pt contamination onto Si surface.

Figure 6 exhibits the amount of adsorbed Pt impurity for 1 hr as a function of alkali additive concentration in UPW containing the 1 ppm contaminant. The contamination in the NH_4OH solution increases with the increase of the concentration; no other solutions (KOH or NaOH) caused the increase of contamination level in the range from ppm to w-% addition into the contaminants. It seems evident that the pH value in Pt containing NH_4OH solution has only a strong influence on the amount of the deposition onto the surfaces.

Figure 7 illustrates the effect of pH value in Pt containing NH_4OH solution on the amount of Pt impurities deposition on silicon surface for 1hr. In order to investigate the influence of the pH in the range between strong acid and alkali, various quantities of HCl or NH_4OH were added into the contaminants with 10 ppm concentration. The pH value in Pt containing solution is proportional to the amount of added NH_4OH. The contamination level on the surface drastically increases with the increase of pH range higher than 9, and being saturated. Following, when HCl chemical is added in the 10000 ppm NH_4OH containing contaminants that maintains a high pH value more than 11 by use of NH_4OH, the amount of contaminants at the same pH range is decreased. The total amount of contaminants on silicon surface seems to depend on pH value in NH_4OH containing the contaminants. Correspondingly, the deposition onto the surface is not possible from the Pt containing aqueous solution in the absence of NH_4OH.

Figure 8 compares the concentration in the Pt contaminant solution *before and after* filtrating through an ion exchange resin such as anion $(R(NR_3)_2(OH)_2)$ or cation

($R(SO_3)_2(H)_2$), which was made on an Inductively Coupled Plasma Mass Spectroscopy (ICPMS) system with a detection limit of ppt level. The pH values in solutions were also adjusted by adding HCl or NH_4OH to Pt contaminant solution. We postulate that the concentration in solution is decreased after filtrating through an anionic ion exchange resin, and hence the Pt contaminants in solution have the negative charge in solution. The Pt impurities in the solution are not deposited to silicon surface, because they cannot take electrons from the substrate. In other words, when the difference of the concentration is a big before and after filtrating the solution by use of cationic ion exchange resin, we suppose that the impurities in the solution still have positive charge on the condition of electronegativity value decrease, compared to that of individual state. Data show that the concentration of Pt impurities has a big difference before and after filtrating through an anionic ion exchange resin, but it is almost same in case of a cationic ion exchange resin. It is, hence, concluded that Pt impurity in solution has negative charge irrespective of pH value, even though it is well known for the metal with electronegativity higher than Si.
On increasing the NH_4OH concentration in Pt contaminant, however, the charge is changed into positive polarity. The Pt impurities in the solution are capable of taking electrons in the Si valance band, so that, the contamination level increases due to the oxidation reduction reaction between Pt ions and Si surface.

CONCLUSION

Various cleaning methods with high ORP value cannot remove the Pt group metals from the Si surfaces, so that, the wafer surfaces should be perfectly separated from the contaminants during process. When the Pt group metals are contaminated onto the surfaces with various chemicals, they are not deposited on the surface in spite of the fact the redox potential of the Pt group metals are much higher than that of Si. In case of the metals containing NH_4OH solution with high pH value, the contamination levels of the Pt impurities only are 2 orders of magnitude higher than those of other impurities (Ir and Ru).

This is attributed to the difference of their ionic state in various solutions. Much more attention should be given for wet chemical selection to prevent the noble metal impurities from contaminating the surfaces.

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This research has been carried out in the Mini Super Clean Room at Faculty of Engineering and in Laboratory for Microelectronics attached to The Electronic Communication Laboratory in Tohoku University.

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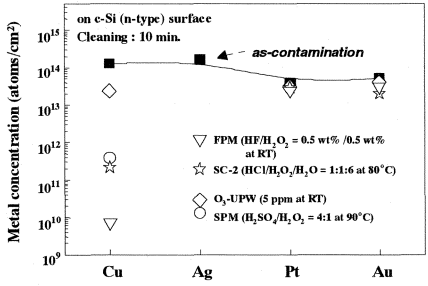

Fig. 1 Noble metals removal efficiency from c-Si surface with various cleanings

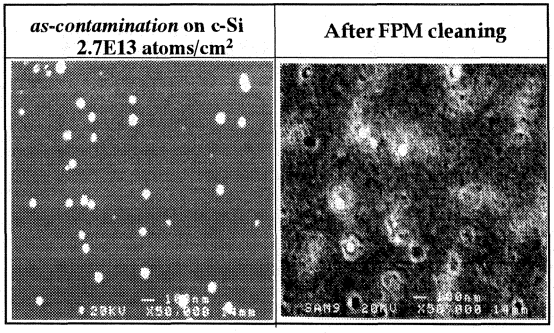

Fig. 2 SEM Photos of *as-contaminated* Pt particles and after FPM cleaning.

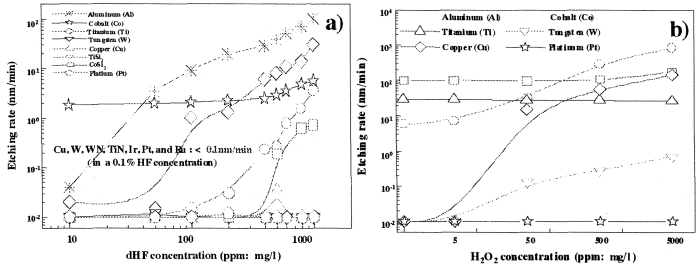

Fig. 3 Various film etch rate of a) dilute HF (dHF) and b) H_2O_2 in a 0.1% HF solutions.

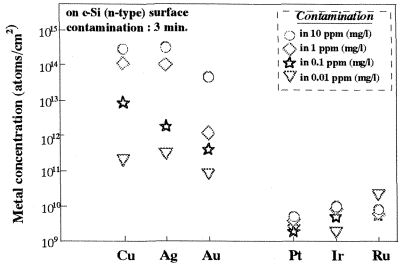

Fig. 4 Noble metals deposition behaviors on c-Si surfaces as a function of varying contaminant concentration.

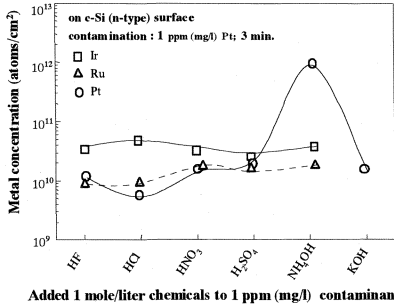

Fig. 5 Dependence of Pt adhesion on c-Si surface with the additive species in contaminants.

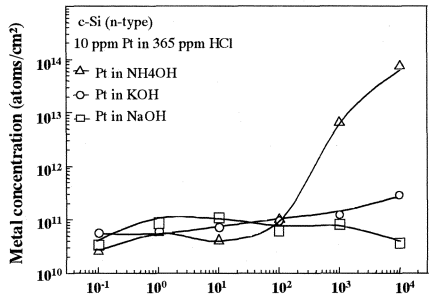

Fig. 6 The effect of alkali additives to the contaminant on Pt deposition behavior.

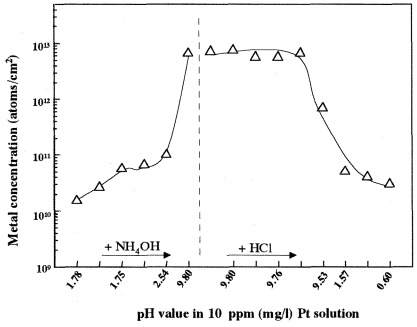

Fig. 7 The Influence of the pH value in Pt contaminants on the amount of deposition on c-Si surface.

Filtration of contaminants containing Platinum (Pt)	Pt concentration (ppm: mg/liter)		
	pH 2	pH 7	pH 10
Before filtrating	1.00	0.97	1.30
Anion ion exchange Filtrating $(R(NR_3)_2(OH)_2)$	**0.01**	**0.01**	**0.07**
Cation ion exchange Filtrating $(R(SO_3)_2(H)_2)$	**0.95**	**0.92**	**1.09**

Fig. 8 The charge characteristics of Pt impurities with pH values.

CO-DEPOSITION MECHANISM OF TRACE Cu AND Fe ON H-Si(100) SURFACE IN BUFFERED FLUORIDE SOLUTIONS

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The mechanism of co-deposition of trace metal ion species onto silicon wafers immersed into aqueous fluoride solution was investigated. It was found that the spontaneous deposition of iron onto the wafer surface was enhanced in the presence of copper for the buffered fluoride solution such as NH_4F. On the other hand, such an effect was not observed for DHF solution. The open circuit potential (OCP) of the wafers immersed in the NH_4F solution possessed further negative potential compared with that obtained with the DHF solution due to higher corrosion rate of silicon surface, indicating the high reducibility for the metallic ions to enhance their deposition. Furthermore, cathodic polarization behavior of the wafers in iron spiked NH_4F solution indicated that the deposition potential of iron shifted toward positive direction in the presence of copper nanoparticles on the wafer surface. The results of anodic stripping voltammetry indicated that the deposited nanoparticles formed alloy of iron and copper. It was suggested that the copper nanoparticles formed on the wafer surface act as catalytic sites for the electron transfer to the iron species under the negative OCP condition, resulting in the enhancement of their deposition.

INTRODUCTION

Wet treatment of silicon wafers with aqueous fluoride solution is a fundamental process for silicon device manufacturing. In this process, spontaneous deposition of trace metal contaminants included in the solutions is one of the critical issues and numbers of studies have been carried out to elucidate its mechanism, mainly focusing upon the deposition processes of single metal species [1-3]. On the other hand, we have found the interaction on the deposition of two trace metal species co-existing in the solution onto H-Si(111) surfaces [4]. We have also investigated the deposition mechanism of trace metals on the silicon wafers as well as the corrosion mechanisms of the wafers in aqueous fluoride solutions [5-8].

Based upon these results, in the present work, interaction effect and co-deposition mechanism of trace metals, such as iron and copper species, on silicon wafer surface in buffered fluoride solution was investigated in detail.

EXPERIMENTAL

P-Si(100) (9-18 Ω cm) and n-Si(100) (18-22 Ω cm) wafers were used in the present work. The wafers were precleaned with a mixture of 4:1 96% H_2SO_4 : 30% aqueous H_2O_2 for 10 min at 120°C, followed by rinsing with ultra pure water. Then they were immersed in 0.5 % aqueous fluoride (DHF) solution (Ultrapur$^{(R)}$ or SLSI grade) for 1 min to prepare clean, hydrogen terminated surface, followed by immersing into the DHF or 40% NH_4F solution (Ultrapur$^{(R)}$ or SLSI grade) containing controlled amount of $Cu(NO_3)_2$ and/or $Fe(NO_3)_2$. The wafers were then observed using a tapping mode atomic force microscope (TMAFM). Amounts of the metals deposited on the wafer surface were measured by radiochemical tracer method [5, 8] using ^{64}Cu and ^{55}Fe species. Electrochemical analyses such as anodic stripping voltammetry (ASV) and open circuit potential (OCP) measurements were carried out for detailed investigation of the interaction mechanism of the trace metal species, using either silicon wafers or a glassy carbon electrode. An Ag/AgCl or SCE electrodes were used as a reference electrode. All the electrochemical potentials shown below are reported with respect to the standard hydrogen electrode (SHE).

RESULTS AND DISCUSSION

Figures 1(a) and 1(b) show representative TMAFM images of n-Si(100) wafers immersed into the NH_4F solution containing either 50 ppb of iron or 20 ppb of copper species, respectively. In these figures, difference in the amounts of deposited metal nanoparticles on the surface can be seen; larger amount of deposits are formed on the wafer immersed into the solution containing copper, whereas few amount of deposits are observed on the wafer immersed in the solution containing iron. As is well known, this can be explained by the difference in the redox potential of the metal species. The potentials for Fe^{2+}/Fe and Cu^{2+}/Cu are -440 mV and +337 mV, respectively; thus the copper possessing noble redox potential forms larger amount of deposits on the surface.

Figure 1(c) shows TMAFM image of the wafer treated with the NH_4F containing 50 ppb of iron plus 20 ppb of copper species. The amount of deposits seems to be larger than simple summation of those seen in the cases prepared from the NH_4F solutions containing single metal species described above.

Such a trend is also observed with p-Si(100) wafers as is seen in Fig. 2, and these are consistent with the previous results by Homma et al. in which trace iron deposition onto Si(111) immersed in NH_4F was enhanced in the presence of trace copper species whereas no significant increase in the deposited amount of copper was ob-

served regardless of the coexisting iron species [4].

Figure 3 shows time dependence of the deposited amount of iron onto the wafer surface in iron spiked NH_4F in the presence or the absence of the copper. It is clearly seen that the amount of the iron linearly increased with an increase in the immersing time in the presence of the copper, indicating the interaction effect of two species.

In the same manner, the wafers immersed into iron, copper, or iron plus copper spiked DHF were observed. However, it was found that the overall amount of the metal deposits was smaller compared with the case with NH_4F solution and the enhancement of iron deposition by copper described above was not seen, suggesting that the enhancement effect is characteristic to the NH_4F solution.

In order to elucidate its origin, various analyses were carried out. Figure 4 shows the dependence of trace copper deposition on the pH of the solutions. As is seen in the figure, the rise in pH increases the deposited amount of copper, which is known as the pH effect. As is seen in Table 1, the OCP for the wafers immersed in NH_4F solution becomes further negative compared with the ones in the HF solutions, which corresponds to previous reports [9, 10], and is thermodynamically negative enough to reduce both copper and iron ions. The OCP can be expressed as

$$E_{(OCP)} = \frac{E_1 + E_2}{2} + \frac{RT}{F} \ln \frac{i_c}{i_a} \qquad (1)$$

where $(E_1+E_2)/2$ corresponds to the averaged thermodynamic potentials of all electron transfer reactions simultaneously occurring at the electrode surface. The i_c and i_a are cathodic and anodic currents corresponding to following reactions;

Cathodic reactions:	$Cu^{++} + 2e^- \rightarrow Cu$	(2)
	$Si_{(s)} + H^+ + e^- \rightarrow Si\text{-}H$	(3)
	$\frac{1}{2}O_2 + H_2O + 2e^- \rightarrow 2OH^-$	(4)
	$H^+ + e^- \rightarrow \frac{1}{2}H_2$	(5)
Anodic reactions:	$Si_{(s)} + OH^- \rightarrow Si\text{-}OH + e^-$	(6)
	$Si_{(s)} + 6F^- \rightarrow SiF_6^{2-} + 4e^-$	(7)

In the case of higher pH solution, the anodic reactions such as Eqs. (6) and (7) are enhanced to increase the corrosion rate of silicon, which pushes the OCP toward negative direction, as is expected from Eq. (1). Such a negative OCP is a driving force to proceed the deposition of metallic species. However, this factor alone cannot explain the "enhancement" of the deposition of iron in the presence of copper. Therefore further investigation is required.

Since it is known that higher overpotential is required for the electrodeposition of iron [11], it is expected that the rate of electron transfer from the surface sites to the iron species plays a key role for the deposition enhancement. Furthermore, Bertagna et al. [5, 12] pointed out that the copper nanoparticles deposited at the silicon surface act as a catalytic sites for the reactions such as hydrogen reduction in aqueous fluoride solution. Based upon these issues, cathodic polarization behavior

of the wafers in iron spiked NH_4F solution was examined. Prior to the polarization, some of the wafers were treated with separate solution containing copper or iron species to form metal nanoparticles at the wafer surface in order to evaluate their catalytic effect on the subsequent deposition process of trace iron.

Figure 5 shows representative cathodic polarization curves for the wafers in the NH_4F solution containing 50 ppb of iron species. The working electrodes are n-Si (100) wafers with either iron or copper nanoparticles on them, which are the same conditions shown in Figs. 1(a) and 1(b), respectively. In this figure, the deposition potential of iron is shifted toward positive direction and the higher current density is observed when the wafer surface has copper nuclei on it, suggesting that the iron deposition is enhanced in the presence of the copper nanoparticles. It is considered that the rate constant for electron transfer leading to the electrochemical deposition of iron is higher on copper nuclei than on silicon surface, which could be one of the origins of the enhancement effect. It should be also noted that the illumination further enhances such a tendency. This seems to be reasonable since the concentration of electrons at the surface is increased by illumination in the case of n-type Si wafers, although detailed investigation is required to elucidate its mechanism.

As described, it is considered that the copper nanoparticles act as catalytic sites for the iron deposition. Since the redox potential of copper is further positive as mentioned above, it is expected that the deposition of copper mainly takes place at very initial stage of the immersion of the wafer into the NH_4F solution containing both copper and iron, and then act as catalytic sites to enhance the iron deposition. By assuming this, it is considered that the deposits form alloy consisting of copper and iron, rather than forming copper and iron particles separately. In order to investigate such a deposition condition, the ASV was carried out. Since the silicon surface is very reactive in the NH_4F solution as described above, glassy carbon electrode was used to focus the interaction between two metallic ion species and to eliminate the effect of silicon surface reactions. First the electrode was maintained at -1060 mV where the deposition of the metallic species were found to take place for 10 min and then the anodic scan was carried out up to +340 mV to observe the profile of anodic currents correspond to the dissolution of the deposits.

Figure 6 shows representative results for the ASV. The anodic dissolution peak for the deposits prepared from the solution containing copper plus iron species shows not the separate peaks which correspond for copper and iron species but the complex feature, suggesting that the formation of an alloy with interacting species. In addition, such dissolution peaks are observed at positive potentials compared with that for their deposition described above, also indicating the formation of alloys.

SUMMARY

In the present work, the mechanism of co-deposition of trace metals onto silicon wafer surfaces in aqueous fluoride solution was investigated. It was found that the deposition of trace iron onto the wafer surface was enhanced in the presence of cop-

per in the case of the NH_4F solution. It is suggested that the copper nanoparticles initially formed on the wafer surface act as catalytic sites to enhance the deposition of the iron under negative open circuit potential of the silicon surface in the NH_4F solution, resulting in the increase in its deposited amount. It is also indicated that the deposits forms an alloy of copper and iron species, which supports this mechanism.

Such an interaction or enhancement effect in the deposition process could be expected to take place for various combination of trace metal species which include copper and other noble species, thus should be an important issue for understanding the overall mechanism of the trace metal contamination in the wet device processes.

ACKNOWLEDGEMENTS

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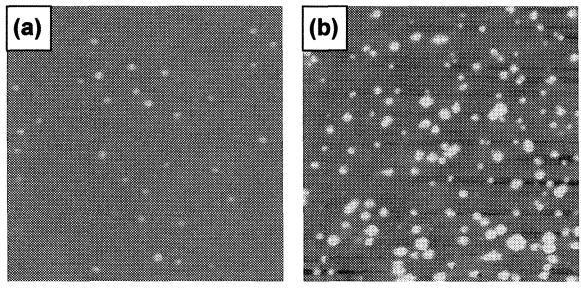

Figure 1 TMAFM images of n-Si(100) wafers treated for 5 min with NH_4F solution containing (a) 50 ppb of $Fe(NO_3)_2$; (b) 20 ppb of $Cu(NO_3)_2$; (c) 50 ppb of $Fe(NO_3)_2$ plus 20 ppb of $Cu(NO_3)_2$. Scan area: 1.0 μm x 1.0 μm; Z scale: 0nm (black) to 40 nm (white).

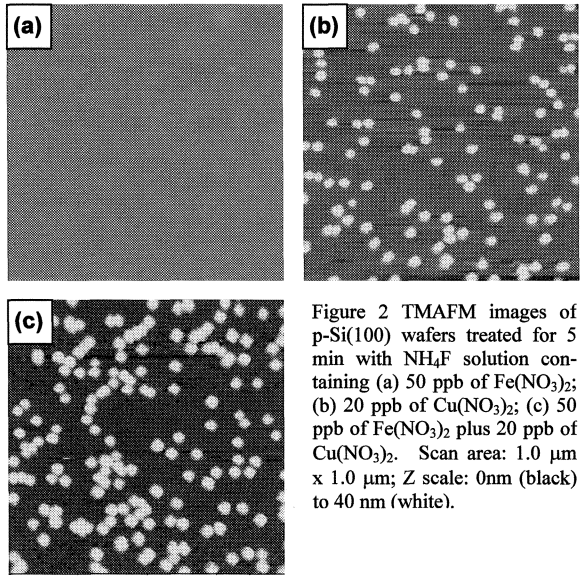

Figure 2 TMAFM images of p-Si(100) wafers treated for 5 min with NH_4F solution containing (a) 50 ppb of $Fe(NO_3)_2$; (b) 20 ppb of $Cu(NO_3)_2$; (c) 50 ppb of $Fe(NO_3)_2$ plus 20 ppb of $Cu(NO_3)_2$. Scan area: 1.0 μm x 1.0 μm; Z scale: 0nm (black) to 40 nm (white).

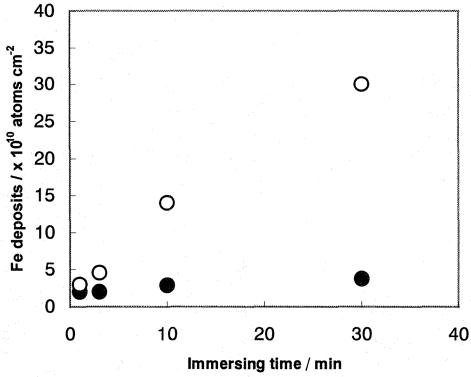

Figure 3 Time dependence of the deposited amount of iron in NH_4F solution containing (●)1.0 ppm of iron species, or (○) 1.0 ppm of iron plus 5.0 ppm of copper species.

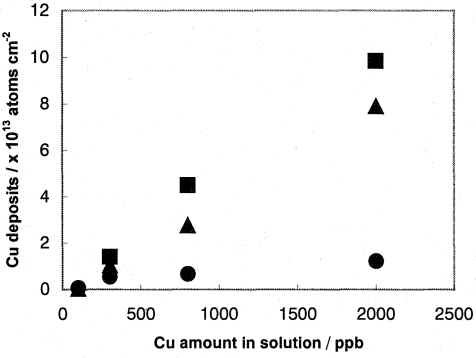

Figure 4 Deposited amount of copper onto p-Si(100) wafer surface from NH_4F based solutions with various pH after 30 sec immersion; (●) NH_4F + HF, pH 6.3; (▲) NH_4F, pH 7.8; (■) $NH_4F + NH_3$, pH 8.8

Table 1 OCP for the wafers in DHF and NH_4F solutions

	OCP / mV vs. SHE	
	n-Si(100)	p-Si(100)
in DHF	-270	-240
in NH_4F	-1180	-1130

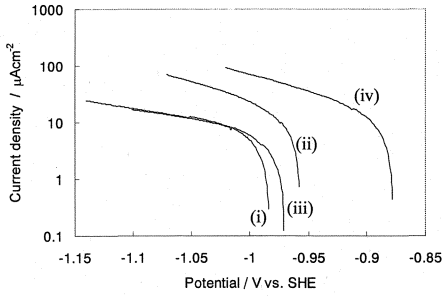

Figure 5 Cathodic polarization curves for (i) iron-deposited, and (ii) copper-deposited n-Si(100) in 40% NH_4F solution containing 50 ppb of $Fe(NO_3)_2$ under dark (0.02 lux) condition. The scans were started from the OCP with the rate of 0.5mV/sec. Curves (iii) and (iv) are obtained with the same wafer and solution condition as (i) and (ii), respectively, with illuminating (55 lux) condition.

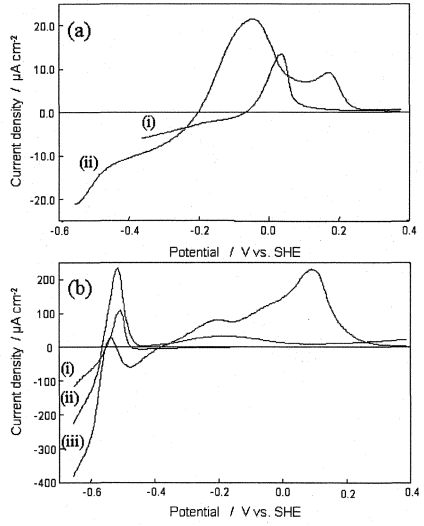

Figure 6 Anodic stripping voltammety profiles of glassy carbon electrode in 40% NH_4F solution; (a) after forming metal deposits at -880 mV for 10 min with (i) pure Cu(II), (ii) Cu(II) + Fe(II); (b) after forming metal deposits at -1180 mV for 30 min with (i) Fe(II), (ii) Fe(II) + Fe(III), (iii) Fe(II) + Fe (III) + Cu(II). Concentrations of metal species: 2.0 ppm.

A STUDY OF METALLIC CONTAMINATION REMOVAL AND ADDITION USING MODIFIED SC-1 SOLUTIONS

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The RCA clean is widely used in the semiconductor industry during various wet-chemical cleaning processes. The RCA clean consists of a particle removal step, the Standard Clean 1 or SC-1 step and a metallic impurity removal step, the Standard Clean 2 or SC-2 step. In this work, we have investigated the addition of chelating agents in SC-1 solutions to (i) prevent metallic deposition and (ii) remove metallic impurities during the SC-1 step, resulting in a very fast RCA replacement clean, opening the door for single wafer wet cleaning.

INTRODUCTION

Although SC-1, a mixture of $NH_4OH/H_2O_2/H_2O$, is an efficient particle removal solution, it inherently allows some metallic impurities in solution to deposit on the wafer surface. For this reason a conventional SC-1 is typically followed by SC-2, a mixture of $HCl/H_2O_2/H_2O$, which exhibits excellent metallic impurity removal efficiency. In aqueous solutions, such as SC-1, a silicon wafer surface is hydroxide terminated (hydrophilic). The interaction of the metal ions in solution and the silanol surface groups can be described by a surface ion exchange mechanism represented by the following equation:

$$\text{-Si-O-H} + M^{x+} \Leftrightarrow \text{-Si-O-}M^{(x-1)+} + H^{+} \qquad [1]$$

Where M^{x+} is the metallic ion. From equation 1, we can see that in SC-1 metal ions in solution tend deposit on the wafer surface under conditions of high pH (low $[H^+]$). The pH dependence of the adsorption for most metals follow this trend and deposit in SC-1 solutions. Al, Fe, and Zn deposit most readily (1). On the other hand, increasing the proton concentration (higher $[H^+]$) or decreasing the free metal ions in solution will tend to remove metallic contamination from the wafer surface (lower $[M^{x+}]$). Unfortunately, acidifying SC-1 will degrade the particle removal effectiveness of the solution. For many years, suppliers have been trying to reduce the free metal ions concentration by the

development and use of ultrapure materials, chemicals, and de-ionized water. Due to the increasingly stringent requirements of wafer cleanliness, this approach is quickly approaching its limitations. To meet and even exceed the current surface metal specifications, it is necessary to not only use ultrapure components, but to add chelating agents to bind free metal ions present forming complexes which will remain soluble in solution. Typical chelating agents can reduce the free metal ions in SC-1 solution by at least 6 orders of magnitude.

An advantage of adding an appropriate chelating agent to SC-1 is to prevent the deposition of metallic impurities during the particle removal step, eliminating the need for a follow-up metallic impurity removal step. Not only does this reduce the number of chemical cleaning steps required, saving money and time, it also avoids the adverse effect of particle re-deposition during typical metallic impurity removal steps, such as SC-2 or dilute HF. An additional benefit of adding a chelating agent to SC-1 is to improve the metallic impurity removal efficiency. A carefully selected chelating agent can provide an "all in one" chemical solution which can clean particles, metals, and organics. Recently, the use of chelating agents in SC-1 based chemistries has gained momentum in the industry (2,3). In fact, such chemistries are now commercially available from several chemical manufactures. The focus of this work is to study the effect on metallic ion deposition and removal by the addition of carboxylic acids to SC-1 solutions.

EXPERIMENTAL

We carried out experiments using a modified SC-1 solution with two concentrations (1:2:40 and 1:2:80 NH_4OH: H_2O_2: H_2O). The concentration of chelating agent was varied from 12ppm to 200ppm. The measured pH value was approximately 9.6. Megasonic energy was applied during the chemical step (power density 1.13 W/cm^2). The process time was 30 or 60 seconds up to 10 minutes at a temperature of 50°C or 80°C followed by a rinse at the same temperature and a spin dry. Two methods of cleaning were studied, immersion and spin cleaning, both in single wafer mode. When used, a HF step consisted of an exposure time of <5 seconds (1:100 HF:H_2O). Additionally, when combined with surfactant, ≤0.2% was used.

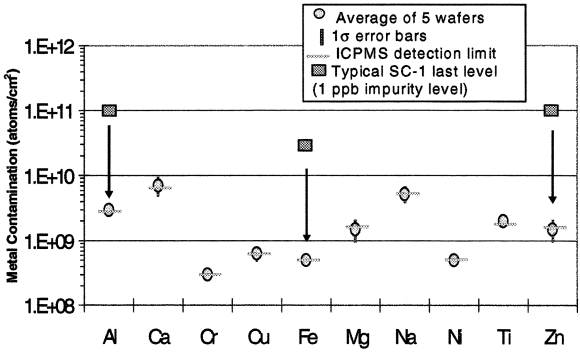
Samples for metal removal experiment were prepared with an immersion method. Wafers were dipped for 10 minutes in a SC-1 solution contaminated with known amount of metals (Fe, Al, Cu, Ni, and Zn). Sample wafers for particle removal studies were prepared with an MSP particle deposition tool. The particle deposition pattern was a combination of full random coverage and a spot. In total, approximately 2300 Si_3N_4 particles with a target size of 0.2μm were deposited on prime 300mm wafers. The particle measurements were performed on a Tencor SP-1.

Surface metal measurements were obtained with the VPD-ICPMS technique. TOF-SIMS was used to assess if any residual chelating agent remained on the surface (after rinsing and drying).

RESULTS

Metal Deposition in Modified SC-1 Solution:

The addition of an appropriately chosen chelating agent clearly reduces metallic ion deposition in SC-1 solutions (Figure 1). In particular, it is interesting to look at the level for Al, Fe, and Zn. These are the metals that readily deposit from conventional SC-1 solutions. For reference, a typical level for a conventional SC-1 clean with a 1 ppb metal impurity level last clean is also shown. All surface trace metals were at or near the VPD-ICPMS detection limits. It is clear that the chelating agent under investigation is efficiently binding the free metal ions in solution reducing deposition onto the wafer surface. Most importantly, the necessity of a SC-2 step can be eliminated with respect to metallic addition.



VPD-ICPMS Det. Limits (1E10 at/cm²)	
Al	0.3
Ca	0.5
Cr	0.03
Cu	0.05
Fe	0.05
Mg	0.1
Na	0.3
Ni	0.05
Ti	0.2
Zn	0.1

Figure 1. Metal Deposition - Surface trace metal level after modified SC-1 clean (single wafer cleaning for 30s @ 80°C).

Metal Removal in Modified SC-1 Solution (Immersion Cleaning):

In order to create a single step RCA replacement solution, it is critical to characterize metal removal as well. It is important that the effectiveness of the modified

SC-1 solution must be equivalent or better than SC-2 solution. Figure 2 shows the surface metal concentration remaining as a function of chelating agent concentration after a 10 minutes (a typical time for immersion cleaning).

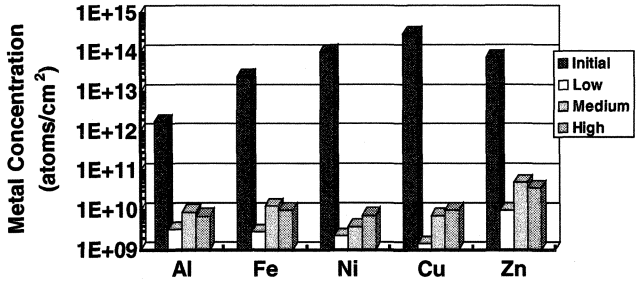


Figure 2. Metal Removal - Surface trace metal level after modified SC-1 clean for different concentrations of chelating agent (immersion clean for 10min @ 80°C).

After 10 minutes, all metals studied were reduced close to or below the 1E+10 level. In most cases this is a 2-4 orders of magnitude of reduction. It is also apparent that the metal cleaning efficiency does not appear to be a function of chelating agent concentration. For short processing times the metal removal efficiency is significantly reduced (Figure 3). After 30 seconds of cleaning, the remaining levels of all metals are higher than for a 10 minute clean. Fe shows a strong dependence on chelating agent concentration, while Al and Zn are only reduced to the 1E +11 level for all concentrations tested. Exposure time is obviously a significant factor for metal removal efficiency.

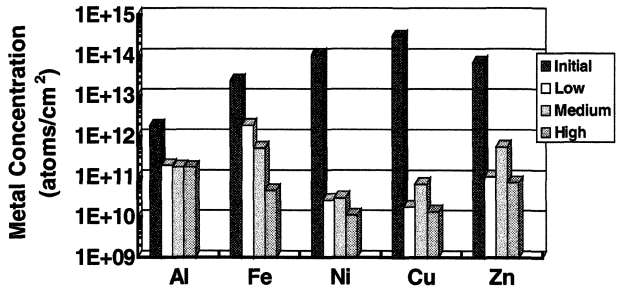


Figure 3. Metal Removal - Surface trace metal level after modified SC-1 clean for different concentrations of chelating agent (immersion clean for 30s @ 80°C).

Metal Removal in Modified SC-1 Solution (Spin Cleaning):

The metal removal results discussed so far have been for immersion cleaning. We also wanted to investigate the effectiveness of modified SC-1 solutions for spin cleaning. Figure 4 and 5 shows the metal removal efficiency for 60 and 30 seconds, respectively.

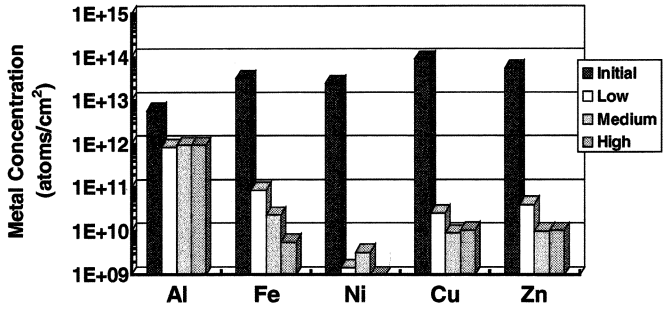


Figure 4. Metal Removal - Surface trace metal level after modified SC-1 clean for different concentration of chelating agent (spin cleaning for 60s).

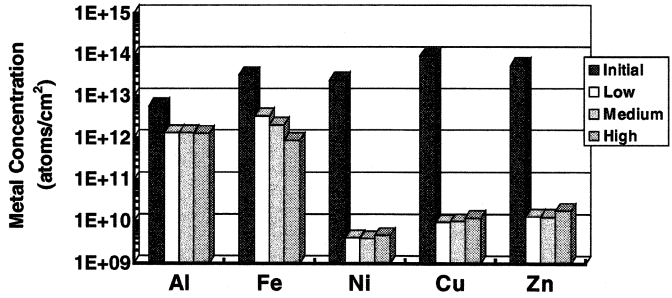


Figure 5. Metal Removal - Surface trace metal level after modified SC-1 clean for different concentration of chelating agent (spin cleaning for 30s).

Figures 4 and 5 clearly show that Fe removal is a function of time and chelating agent concentration. Although Ni removal is quite easy, the removal is greater for 60 seconds. It is interesting to compare a Figure 3 (30s immersion clean) and Figure 5 (30s spin cleaning). Although both Al and Fe are poorly removed in 30 seconds, immersion cleaning performs slightly better than spin cleaning. On the other hand, for metals that are generally easier to remove, such as Ni, Cu, and Zn, spin cleaning outperforms

immersion cleaning. In any case, the effectiveness of the modified SC-1 to remove metals can be realized for both immersion and single wafer cleaning methods.

In addition to chelating concentration the effect of temperature was also studied (for shorter processing times only). The temperature levels studied were 50°C and 80°C, typical boundaries for SC-1 cleaning. For equivalent chelating concentrations 80°C was much more effective for metal removal than 50°C (Figure 6).

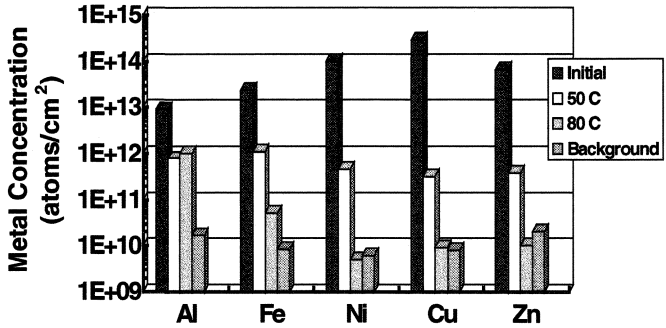


Figure 6. Metal Removal - Surface trace metal level after modified SC-1 clean for different temperatures (spin cleaning for 60s).

All metals studied were reduced by more than order of magnitude by increasing the temperature to 80°C, with Al as the exception.

All of the results clearly show that the removal of Al is a key challenge. In SC-1 solutions, Al has been shown to deposit on the wafer surface, but also to be partially included in the chemical oxide (4). The only way to remove Al with a modified SC-1 solution is to partially etch the chemical oxide. The amount of chemical oxide etched for a 30 second exposure to the modified SC-1 solution was measured to be <1Å. Although a small amount of etching during cleaning is a technological advantage for fabricating dual and triple gate structures (conventional SC-1 cleans etch 5-50Å), it does not etch sufficiently to remove Al from chemical oxide. This explains the difficulty for the modified SC-1 solution to remove Al for short exposure times.

As the concept of single wafer technology requires fast processing to reduce cycle time, it was apparent that a small amount of etching was necessary to remove all surface metals faster. In order to improve the Al removal for short process times we investigated the use HF to slightly etch the top surface layers of the oxide. Figure 7 illustrates the effectiveness of this approach. Not only is the Al removal improved, such a cleaning sequence can reduce all metal levels to 1E+10 level in under 30 seconds. The most robust processing sequence is HF followed by modified SC-1. This process also resulted in the lowest surface metal levels for all of our testing. The HF step will efficiently

remove most of the metal contamination (Cu being the exception), and the SC-1 with chelating agent will effectively remove the remaining Cu and prevent metal deposition from solution. The HF followed by modified SC-1 last process sequence provides a very efficient particle and metal clean.

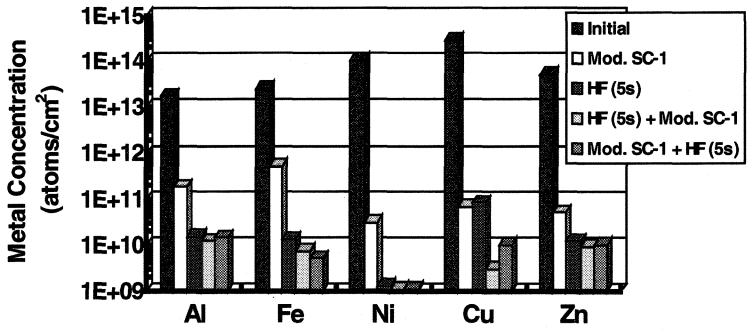


Figure 7. Metal Removal - Surface trace metal level after modified SC-1 clean for different temperatures (single wafer clean for 60s).

The addition of a HF step clearly improves the metal removal efficiency for all metals for very short processing times. It should be noted that the amount oxide etched for the sequence was very small ~2-4Å. This result also supports the conclusion of M. Tsuji *et al.* (4) that small percentage of Al is in fact incorporated in the near surface chemical oxide when immersed in contaminated SC-1 solutions (containing Al).

One of the concerns with the use of chelating agents and or surfactants in SC-1 last cleans is the potential of organic contamination remaining on the surface of the wafer. However, in modern wet cleaning equipment, the rinse process can be optimized to eliminate such concerns. The use of heated DI water rinse and high spin rates during rinsing can effectively remove all traces of the chelating agent. TOF-SIMS measurements were carried out to confirm the absence of the both the chelating agent and surfactants (when used). No trace of chelating agent or surfactant specific residues was observed on the processed wafers (5,6).

Finally, as a check we confirmed that the particle removal efficiency of the optimized chemistry. For one lot, consisting of 13 wafers, the average particle removal efficiency was 99.5% (1σ=0.28%; measured at $\geq$ 0.12μm). The particle cleaning performance for the modified SC-1 solution was excellent.

CONCLUSIONS

In this paper we have shown that an appropriately chosen chelating agent can prevent metal deposition SC-1 solutions. When combined with a slight HF etch, the modified SC-1 solution can effectively remove metal contamination to less than 1E+10 in less than 30 seconds. It was also shown that an optimized process can easily rinse away any chelating agent and surfactant residue. The most robust process sequence with regards to particles and all metals (including Cu) is HF followed by modified SC-1.

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MICRO-CONTAMINATIONS OF COPPER AND SILVER ON SILICON WAFER SURFACES

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Micro-contaminations of copper and silver on n-type silicon wafer surfaces were investigated by performing a series of electrochemical polarization measurements in 5% hydrofluoric acids and ethanol solutions in the absence and presence of various concentrations of copper and/or silver. The metallically contaminated wafer surfaces were characterized by scanning electron microscopy (SEM). It was revealed that the open-circuit potentials shifted to a more anodic direction and the corrosion current densities significantly increased when either copper or silver was present in solutions, and these became more pronounced when both copper and silver were simultaneously introduced into solutions. The polarization resistance showed a sensitive linear decrease with an increase of copper or silver concentrations, a strong indication of an accelerated electrochemical reaction. The contaminated wafer surfaces were covered by metallic nano-crystallites due to copper and silver deposition from solutions. When both copper and silver were present, the nano-crystallites tended to be coagulated each other and various clusters were formed by combing metallic atoms. As the concentration of copper and/or silver became larger, the amounts of metallic nano-crystallites remarkably increased, this in turn further promoted metallic micro-contaminations and ultimately led to rougher wafer surfaces.

INTRODUCTION

Metallic contamination in silicon represents one of the major causes for low yields and poor performance of semiconductor devices. Transition metals with rapid diffusion in silicon such as copper, iron, and nickel, have deleterious effects on device characteristic[1]. Trace amounts of noble and transition metals such as gold, silver and copper dissolved in dilute hydrofluoric acid (HF) or buffered HF solutions tend to contaminate wafer surfaces by plating out from solutions during wet cleaning and etching processes[2-7], while iron and nickel contaminants are found not to be deposited onto silicon surfaces[8-9]. Although single metallic contamination has been extensively studied with particular attention being paid on copper due to its wide presence in IC fabrications and serious contamination for silicon devices, contaminations involving two or more than two metals have not yet been

probed so far. In fact, contaminations from metals other than copper such as silver, iron and nickel often occur simultaneously in device manufacturing. It is, therefore, important to identify multiple metallic contaminations and furthermore to understand their behaviors.

In this work, micro-contaminations of copper and silver on n-type silicon wafer surfaces were investigated individually or jointly by performing a series of electrochemical polarization measurements in 5% HF and ethanol solutions. Various concentrations of copper and silver were intentionally added into the solutions. The nature of copper and silver micro-contaminations was studied by analyzing electrochemical behaviors of silicon, and the morphologies of metallically contaminated wafer surfaces were obtained by scanning electron microscopy (SEM).

EXPERIMENTAL

The silicon wafer samples used in this study were n(100) single crystal with a resistivity ranging 2~4 Ω·cm. The chemicals used were of ultra-pure analytic grade. Different concentration levels of copper and silver were prepared by diluting from 1000 ppm Cu^{2+} and Ag^{+} standard solutions (in HNO_3), respectively, down to the desired values. The electrochemical cell body was made of Teflon. The working and counter electrodes were silicon wafer and platinum flake, both were held vertically and facing each other. The exposed area of silicon to electrolytes was fixed at 1 cm^2. The reference electrode was saturated calomel electrode (SCE). All the tests were performed at room temperature and under normal room light condition.

Electrochemical polarization measurements were carried out using an EG&G model 273A Potentiostat in 5% HF and ethanol solutions in the absence and presence of various concentrations of copper or/and silver. The cleaning and drying procedures of wafer samples before measurements were the same as previously described[7]. The morphologies of metallically contaminated wafer surfaces were studied by SEM technique using a Hitachi S-520 scanning electron microscope. The accelerating energies ranged 20~25 KeV. All the samples were examined by SEM without coatings.

RESULTS AND DISCUSSION

Typical polarization curves of n-type silicon in 5% hydrofluoric acid and ethanol solutions containing different concentration levels of copper and silver indicated on each curve are shown in Fig. 1, respectively. The curve labeled as "blank" was obtained in the solution without intentionally adding copper and silver for comparison. It is evident from the figures that in both cases the open-circuit potentials shifted to a more anodic direction and the corrosion current density, which is a direct measure of electrochemical reaction rate, increased considerably when either copper or silver was individually added into solutions.

It is generally believed that in dilute HF solution silicon is subject to anodic dissolution which causes surface roughness, while hydrogen evolution is the possible cathodic reaction accompanying silicon dissolution.

$$Si + 6HF \rightarrow H_2SiF_6^{2-} + 4H^+ + 4e \quad (1)$$

$$2H^+ + 2e \rightarrow H_2 \qquad E^o = 0.00\ V \quad (2)$$

In the presence of copper or silver, metal deposition will take place and compete with hydrogen evolution.

$$Cu^{2+} + 2e \rightarrow Cu \qquad E^o = 0.34\ V \quad (3)$$

$$2Ag^+ + 2e \rightarrow 2Ag \qquad E^o = 0.80\ V \quad (4)$$

Previous related studies indicate that hydrogen evolution (Reaction (2)) was actually enhanced by copper deposition[6-7]. Hence, the silicon oxidation (Reaction (1)) is accelerated since redox potentials of silver and copper deposition are more anodic than that of hydrogen evolution, implying that either copper or silver is more readily reduced than hydrogen. The deposition of copper and silver from solutions also leads to changes in cathodic slopes, variations in corrosion current densities and open-circuit potentials as evident in Fig. 1. In the absence of metallic contamination (the curve indicated as "blank" in Fig. 1), the cathodic slope of n-type silicon showed a typical linear behavior corresponding to Reaction (2). When either 1 ppm copper or silver was intentionally added

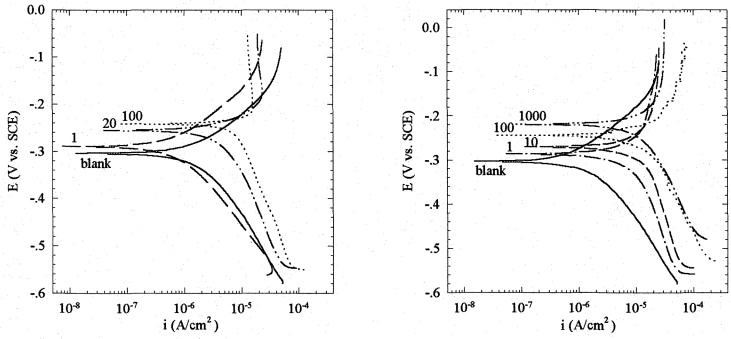

Fig. 1 Typical polarization curves of n-type silicon in the absence and presence of metal contaminants (a) copper and (b) silver (Numbers on each curve indicate the copper or silver concentrations in ppm)

into the solution, the polarization curve shifted to a more anodic direction, and the corrosion current density notably increased. As the contaminant concentrations further increased, these became more pronounced.

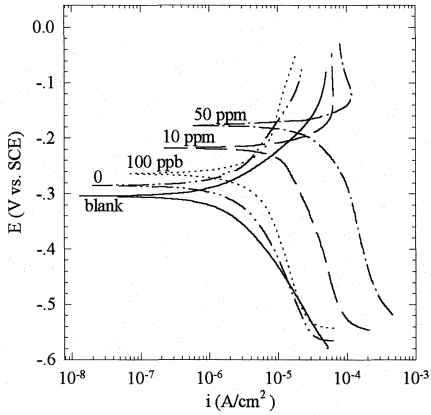

Fig. 2 Polarization curves of n-type silicon in solutions containing 100 ppb silver and various copper concentrations indicated on each curve

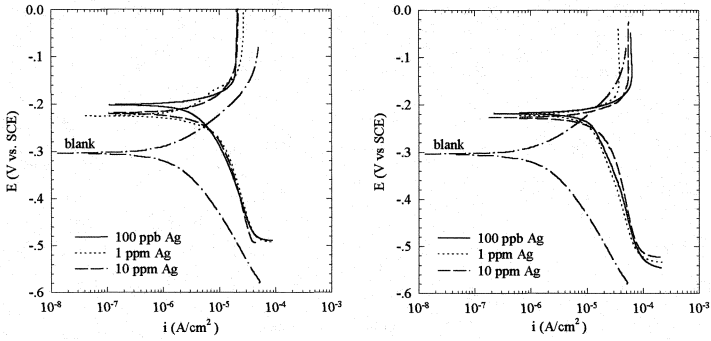

Fig. 3 Polarization curves of n-type silicon in solutions containing various concentrations of copper and silver contaminants (a) 1 ppm copper with variation of silver (b) 10 ppm copper with variation of silver

In an effort to investigate the nature of micro-contaminations of copper and silver when they are simultaneously present in solutions, polarization curves were measured in solutions containing 100 ppb silver with variations in copper concentrations, and the results are given in Fig. 2. For a comparison polarization curve obtained without intentionally adding copper and silver contaminants (indicated as "blank" curve) is also included in the figure. When trace amount of silver (100 ppb) was initially present in solutions while no copper was added (Curve labeled as "0"), the curve shifted to a more anodic direction and the reaction rate increased due to silver deposition. The additions of copper into solutions containing 100 ppb silver further promoted the corrosion rate and increased the open-circuit potential. The cathodic slope became steeper.

Polarization curves were also obtained in solutions containing 1 ppm and 10 ppm copper, respectively, and various silver concentrations as provided in Fig. 3. If either 1 ppm or 10 ppm copper was initially present in solutions, the addition of trace amount of silver (100 ppb) also significantly increased the corrosion rate and the open-circuit potential similar to what were observed in Fig. 2. However, further additions of silver into solutions containing 1 ppm or 10 ppm copper appeared to have minimal effects on the polarization responses. This suggests that copper will more detrimentally influence the wafer surface in silver-contaminated solutions than silver in copper-contaminated solutions. The following reaction is thermodynamically possible to occur when both copper and silver are simultaneously present in solutions.

$$Cu + 2Ag^{+} \rightarrow Cu^{2+} + 2Ag \qquad (5)$$

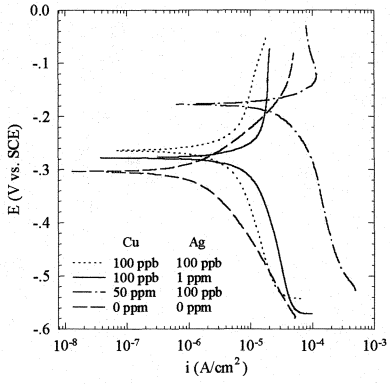

Fig. 4 Polarization curves of n-type silicon in the absence and presence of various concentrations of copper and silver contaminants

The concentrations of Cu^{2+} and Ag^{+} in solutions are critical to metal deposition as indicated by Reaction (5). If Cu^{2+} is initially present at a concentration higher than Ag^{+}, copper deposition takes place more favorably and becomes predominant; slightly increasing Ag^{+} concentration would not effectively affect copper deposition. Similarly, if Ag^{+} concentration is initially larger than Cu^{2+} concentration, silver deposition occurs preferentially, copper deposition takes place only when Cu^{2+} concentration is much higher than Ag^{+} concentration. These are consistent with the polarization behaviors observed in Fig. 2 and Fig. 3.

To further clarify the electrochemical nature of copper and silver deposition on n-type silicon, more polarization curves were obtained through electrochemical measurements, and the results are illustrated in Fig. 4. The dashed line in the figure represents the polarization response observed in "clean" situation (no metal contaminants were intentionally added), which exhibits typical Tafel slops on both anodic and cathodic branches. The dotted line was recorded when both 100 ppb copper and 100 ppb silver were simultaneously added into solutions. The accelerated reaction rate was apparent with larger corrosion current density and the steeper cathodic slop. The solid line denotes a case for larger silver concentration and smaller copper concentration, while the solid-dot line denotes larger copper but smaller silver concentrations. As compared the solid line with the dotted line (a case for equal amounts of copper and silver additions), slight increase in the corrosion rate was observed when silver concentration changed from 100 ppb to 1 ppm. By comparing the dotted line with the dot-solid line, the increase in copper concentration from 100 ppb to 50 ppm significantly enhance the corrosion rate. Evidently, simultaneous additions of copper and silver into solutions more pronouncedly affected the reaction rate, in particular with high concentrations of both copper and silver; accordingly, the wafer surfaces became more seriously contaminated.

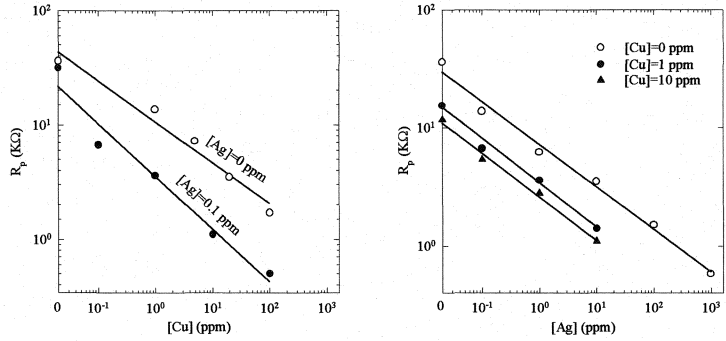

Fig. 5 Polarization resistance as a function of copper and silver concentrations in solutions (a) copper (b) silver

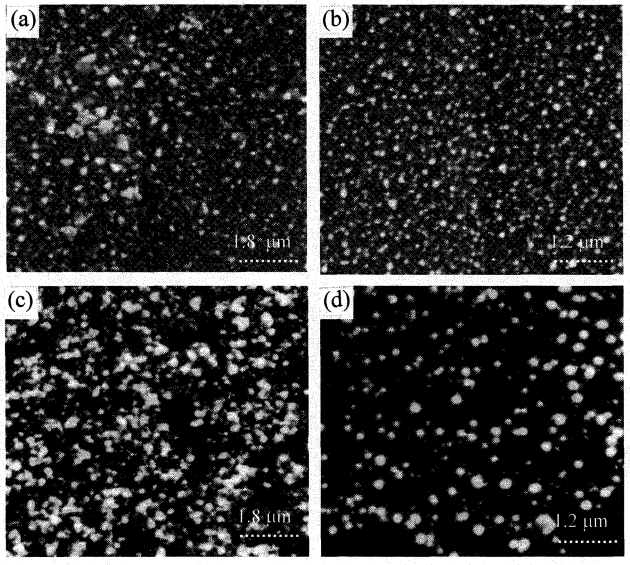

Fig. 6 Micrographs of metallically contaminated silicon wafer surfaces (a) 10 ppm copper (b) 100 ppm silver (c) 10 ppm copper and 1 ppm silver (d) 1 ppm copper and 10 ppm silver

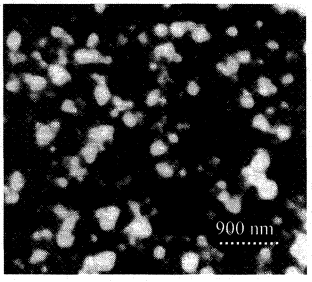

Fig. 7 Micrograph of contaminated silicon wafer in solutions containing 10 ppm copper and 1 ppm silver showing various clusters by combining metallic atoms

The polarization resistance (R_p), which is an inverse of electrochemical reaction rate, can be calculated from each polarization measurement and is plotted against copper or/and silver concentrations on a logarithmic scale in Fig. 5. A linear decrease with an increase of contaminant concentrations is observed no matter whether copper and silver are individually or simultaneously present in solutions. The values of R_p dropped rapidly as copper and silver concentrations increased, indicating an accelerated reaction at the silicon/solution interface. The values of R_p obtained when copper or silver was individually present in solutions were smaller than those obtained when both copper and silver were added into solutions. This re-confirms that more serious metallic contamination occurred when both copper and silver were simultaneously present in solutions.

Surface morphologies of copper or/and silver contaminated silicon wafer samples are compared in Fig. 6. The SEM micrographs clearly showed the deposited nano-metallic crystallites. It is evident that the wafer surfaces became rougher as copper and silver nano-crystallites were deposited from contaminated solutions. When both copper and silver were present in different concentrations (Fig. 6(c) & (d)), the nano-crystallites tended to be coagulated each other at the wafer surfaces, various clusters were formed by combining metallic atoms, and this became more pronounced in the case of larger copper smaller silver concentrations (Fig. 6(c)). Fig. 7 provides strong evidence for the formation of clusters and reveals the detailed features of clusters with a more expanding view of Fig. 6(c). Copper and silver micro-contaminations produced larger amounts of nano-crystallites than single copper or silver contamination did, leading to heavier formation of clusters at the wafer surfaces.

CONCLUSION

It was demonstrated from this study that electrochemical polarization measurements were sensitive to different levels of copper or/and silver contaminations on wafer surfaces, as strongly indicated by a linear decrease in polarization resistance with an increase of contaminant concentrations. In addition, anodic-shifting in open-circuit potentials and increase in corrosion current densities were also observed from polarization curves. It was also found that copper had more detrimental effect than silver when both were simultaneously present in solutions. Single copper or silver contamination mainly caused the deposited nano-crystallites being more deeply diffused into silicon substrates and resulted in rougher surfaces, while micro-contaminations of copper and silver produced heavier clusters on wafer surfaces by combining metallic atoms in addition to metallic diffusion, which ultimately led to more serious contamination.

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IONIC CONTAMINATION OF THE SILICON WAFER FROM WAFER CLEANING PROCESS

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A number of anions and selected water-soluble cations have been investigated following their deposition from sulfuric-peroxide mixture (SPM) process and subsequent removal by DI water rinsing and dilute SC1 processes. Particular attention has been paid to sulfate anion. The objective of the current study is to evaluate the factors affecting removal of these ions from the wafer surface following SPM process. The surface concentration of the anions and cations on the wafer surface was identified with ion-chromatography (IC). A number of observations have been made regarding rinse characteristics of these anions and cations. The information can be used to control ionic contamination and optimize RCA based cleaning process. Additional benefits include reduced water and chemical consumption, reduction of cycle time with higher wafer throughput that results into lower cost of ownership.

INTRODUCTION

Control of ionic contamination of the silicon wafer is important for the prevention of haze, organic contamination, particle contamination, metallic contamination and metallic corrosion. Better understanding of the deposition and rinse behavior of the ionic contamination is important for optimizing the overall cleaning process.

A number of anions including sulfate and selected water-soluble cations have been investigated following their deposition and subsequent removal by DI water rinsing and dilute SC1 processes. Particular attention has been paid to sulfate anion. However, rinse behavior of other anions and selected cations are also indicated. SPM is probably one of the best oxidants used in wet processing of wafer. It was originally introduced to remove photoresist from surfaces but now in most cases that is done by ashing (plasma). SPM is still used for organic and resist removal.

However, the resist removal is pursued only when the structure on the wafer surface is believed or proven to be susceptible to plasma damage. However, the ashing processes are not perfect and can leave residual resist or carbonized resist, especially if the resist has been used as a mask for implantation. Furthermore, it may still contains metallic contaminants that will be concentrated on the surface when the resist is ashed off. So additional wet process is needed to clean such surface.

SPM is frequently used, at temperatures of 120°C, to remove organics from wafer surfaces in the semiconductor industry [1]. Because of the high viscosity of the mixture, even at elevated temperature, it takes significant large volume of rinse water to lower the concentrations of residual anions and cations. Furthermore, surface chemistry studies of the standard SPM solutions reveal that these solutions tend to be chemophilic implying the attractive behavior of the ion species to the wafer surfaces during and after immersion in a process tank [2]. Additionally, high level of residual sulfate anion known to produce excessive light-point-defect (LPD) on wafer surface when stored in cleanroom environment [3]

The objective of the current study is to evaluate the factors affecting removal of these anions from the wafer surface following SPM process. Silicon wafer processed in SPM solution subsequently rinsed either with hot DI water or hot DI water followed by dilute SC1. Variation of ion rinse efficiencies as a function of rinse type, immersion times in sulfuric acid and rinse parameters are investigated in the present study. In addition, some of the wafers treated with sulfuric acid and rinsed were exposed to the cleanroom environment to allow for particle growth from residual contamination. It is a challenge and often beneficial to develop optimized rinsing processes that include but not limited to better performance, reduced water consumption, shorter cycle times, higher tool utilization, and higher throughputs. This was verified experimentally using an automated wet tool. The information can be used to control ionic contamination and optimize RCA based cleaning process.

EXPERIMENTAL

The experimental setup was conducted with 8-inch n-type bare silicon wafers (resistivity 14-20 ohm-cm) with chemical mixture of sulfuric acid and hydrogen peroxide at a ratio of 6 : 1. Spiking of the mixture with hydrogen peroxide was done at an interval of 240 ml every hour to minimize wafer surface etching. Following SPM treatment wafers were rinsed either with hot DI (50 C) water or hot DI water followed by dilute SC1 (1:2:100) at 50 C. They were subsequently dried in IPA vapor in an automated wet bench with 50-wafer cassette. The temperature of the chemical bath was kept constant at 120C and the residence times were 5 and 10 minutes. Both the SPM and the SC1 processes are carried out in a recirculated bath employing 0.1micron chemical filtration. Rinsing process included quick dump rinse (QDR), overflow rinse (OFR), and combination of both modes to examine the residual sulfate ion (SO^{-2}_4) other ions on bare silicon wafers. Multiple QDR were employed with 60 seconds duration between the dumps.

Approximate OFR flow rate used here is 13 gallons per minute (gpm). The test matrix involved fourteen different test runs as shown in Table 1 and was carried out using SCP-E200 automated wet bench linear tool. The variables studied here were number of quick dumps, retention time of bare silicon wafers in SPM chemistry, and rinse time in overflow rinse tank. Pre and post particle measurements were determined using the KLA

Tencor TBI. Water leachable anions and cations from wafer surfaces were determined by Ion Chromatography (IC). Residual SPM contaminants resulting into growth of particle on wafer surface after the wafers have been exposed into clean room environment, for 31 hours, were measured with KLA Tencor TBI. Measurement of anions and cations in the DI water is made using ion-chromatography close to the point-of-use.

RESULTS AND DISCUSSIONS

The effect of process parameters on the rinse and particle level on the wafers is provided below with the discussion.

Residence Time in SPM Bath

Multiple experiments with different retention time in SPM bath. This is shown in Table 1. Run #s 1 through 6 were conducted with 10 minutes retention time while runs 7 through 14 were retained for 5 minutes in the chemical bath. Only OFR is used for run # 13 and run #14. The corresponding amount of residual sulfate anion on the wafers are shown in Table 2.It was observed that the longer bare silicon wafers are exposed to the SPM mixture the more SO_4^{2-} anions are on the wafer surfaces after the rinse step. Overflow rinse time has some impact on the residual sulfate ions on the wafer. However, increasing the number of QDR reduced the amount of residual sulfate on the wafer for both 10-min and 5-min. duration of wafer in SPM bath. Average particle level on the wafer following similar amount of rinsing is less with 5-min SPM compared with 10-min. SPM residence time. This indicates a higher level of residual contaminants remain on the wafer when exposed to longer period of SPM. Furthermore, the rinse rate of the wafer is higher for 5-min. chemical treatment compared to 10-min chemical treatment and can result into reduced water usage for depending on the process requirement.

Ion Level following DIW Rinse

The level of selected anions and cations on the wafer surface as measured by ion chromatography for the different process conditions, indicated in Table 1, is provided in Table 2. Only selected ions are indicated here, though a number of additional anions and cations are measured. Detection limits for the anions varied between 1.0 to 2.5 E+11 atoms/cm^2 and is lower than the detection limits for cations. The detection limits for the cations by IC is nearly twice that of the anions. It is also expected that there are some variations in percent recovery of the each individual ion by DI water. The levels of anions and cations on the control wafer are shown in the same table. Following observations can be made with regard to the effect of rinsing on these anions as shown in Table 2.

The level of sulfate ion on the wafers is increased significantly following treatment of the SPM process. The residual sulfate level tends to increases with the increased retention time in the SPM bath. Additional rinsing do not significantly alter the level of sulfate on the wafer. The sulfate level in the rinse water was below the detection

limits of 50 ppt. Increased retention time in SPM bath results into higher level of nitrate ion in water. However, additional rinsing tends to lower the residual nitrate ion from the surface of the wafer. The nitrate level in the rinse water is below the detection limit of 20 ppt.

The concentration of the nitrite ion on the wafer surface is increased by nearly 2-3 times that of the initial concentration and is independent of the residence time in the SPM bath. This indicates a partial recontamination of the nitrite ion by the rinse DI water. The level of nitrite ion in the water is below the detection limit of 20 ppt.

The level of chloride ion on the wafer surface is decreased following rinsing for each of the processes. This indicates that the DI water is effective in reducing the chloride ion. The level of chloride ion in the rinse water is 30 parts per trillions (ppt).

The level of fluoride on the wafer surface is nearly 3-5 times the level of fluoride on the control wafer. Increased retention time in SPM and rinse water tend to increase the residual fluoride ion on the wafer surface. It is possible that the chemophilic nature of sulfuric treated surface trapped fluoride ion, present in DI water, on the wafer. The level of fluoride ion in rinse water is less than its detection limit of 100 ppt.

Among the cations only the level of sodium and ammonium ions are shown in Table 2. Sodium ion is highly soluble in DI water. The level of sodium on the wafer controls the level of sodium ion on the wafer surface. The level of sodium in the rinse DI water is less than its detection limit of 7 ppt. Ammonium ion tends to increase following treatment of sulfuric acid. Again the rinse water is likely the source of increased level of NH_4^+ observed on the wafer surface. The level of ammonium ion in DI water is less than its detection limit of 50 ppt.

Additional ions like bromide, phosphate, lithium, magnesium and calcium are also measured. The levels of these ions are low and unaffected by the rinse process following sulfuric acid treatment. Residue of these ions on the wafer is considered to be in equilibrium to the amount present in rinse DI water. It is important to realize that the amount of ionic level in DI water though measured near point-of-use but might not be same in the rinse bath. The amount of ions in the rinse water bath is normally more than that indicated here. The equilibrium contaminants on the wafer surface are more closely related to level of ions present in DI water rinse bath.

Ion Level following SC1 rinse

In a separate experiment the SPM treated wafers were first treated with SC1 solution followed by DI water rinsing. The process sequence is shown in Table 3. The corresponding residual ions on the wafer surface are shown in Table 4. From Table 4 it is observed that the level of sulfate ion on the wafer is reduced by more than an order. Recontamination of wafer from other ions was kept at a minimum level except for

chloride ion that showed a small increase. From this observation it can be concluded that SC1 process cleans up effectively residual sulfate anions. Furthermore, the nature of the surface and the chemical oxide following SC1 process tends to maintain low ionic contamination. The level of other leachable ions, such as bromide, phosphate, calcium and magnesium were unchanged with SC1 treatment.

Furthermore, we also observed better particle performance on wafer following SC1 rinse compared to rinse without SC1 as expected. This particle addition on the wafer following SC1 cleans is found to be inversely related to the OFR rinse time. OFR time was varied between 2 to 14 minutes following same number of QDR rinse in each case. Particle level reaches a minimum at about 12 minutes of OFR. This is shown in Table 5. The result clearly indicates the benefit of OFR following QDR.

LPD Growth in Cleanroom Environment

Residual sulfate anion known to produce excessive light-point-defect (LPD) on wafer surface when stored in cleanroom environment [3]. Experimental results correlate with investigation [4] indicating that growth of light-point-defect (LPD) on wafer immediately following an SPM clean. Figure 1 shows LPD growth for particle sizes ≥ 0.16μm with OFR times of 1, 2, and 4 minutes, at constant QDR time of 5.5 minutes, after 31 hours of exposure in a class-10 clean room. From Figure1 it is seen that particle level is decreased as OFR time is increased. In our data, shown in Table 2, we have not seen a significant variation in residual sulfate concentration with increase in OFR time. However, there might be some uncertainty in the measurement of leachant ions. Furthermore, variation in sulfate concentration of the starting materials might have resulted into lower level of sulfate concentration on the actual wafers during this rinse experiment. An empirical fit to the particle growth rate data is shown in Figure 2.

CONCLUSION

The chemical composition of wafer surface after SPM clean depends on the chemical solutions and process conditions used to perform the clean. The results discussed show that the amount of deionized water rinse in conjunction with the rinse type played an important role in determining the amounts and nature of surface impurities. In this study the post-SPM wafer surfaces were characterized for particles and leachable ionic impurities. Incomplete rinsing following SPM treatment results into particle and sulfate ionic densities on wafers. Particle adders are reduced with additional rinse time (QDR) followed by longer OFR rinse. Residual sulfate ions from inadequate rinsing act as a trap for both ionic contaminants [5] Further rinsing tends to reduce the level of these impurities. The results from this study show that a reduction of SO_4 anions on the wafer surface with reduced retention time and particularly with SC1 treatment for SPM treated wafer. A quantitative understanding is provided about the dynamics of ionic contamination and their subsequent removal by different rinse processes. This information can be combined with conductivity measurement of the rinse water to

develop process specific rinsing process. Based on the process tolerance for ionic contamination, hot DI water rinse for water at low ionic contamination can be used to optimize RCA based wafer cleaning process. Benefits from such process improvement include reduced water and chemical usage, reduction in cycle time. This in turn will result into higher throughput and lower cost of ownership for wet cleaning process.

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Table 1. Process conditions and sequence for SPM treatment studies

Test Run #	Chemistry	QDR	OFR, min.	Wafer Retention in SPM Bath, minutes
1	SPM 6 : 1 120C	4 Dumps	1	10
2		4 Dumps	2	10
3		4 Dumps	4	10
4		6 Dumps	1	10
5		6 Dumps	2	10
6		6 Dumps	4	10
7		4 Dumps	1	5
8		4 Dumps	2	5
9		4 Dumps	4	5
10		6 Dumps	1	5
11		6 Dumps	2	5
12		6 Dumps	4	5
13		NO QDR	11	10
14		NO QDR	12	10

NOTE: An untreated wafer was set aside as control wafer.

Table 2: Ion Chromatography data for selected anions and cations concentration on wafer surfaces after SPM clean and rinse steps from Table 1.

Test Run #	Anions (x 10^{11} atoms/cm^2)					Cations.(x 10^{11} atoms/cm^2)	
	F^-	Cl^-	NO_2^-	NO_3^-	SO_4^{-2}	Na^+	NH_4^+
Control	3.1	12	<2.0	8.3	<1.0	4.9	48.0
1	8.4	5.2	6.3	30	50	<2	110
2	13	4.5	7.2	33	50	<2	110
3	16	4.0	5.9	6.7	47	2.9	77
4	17	2.8	13	5.2	32	<2	93
5	14	4.4	4.3	5.6	27	3.5	61
6	15	4.5	7.4	7.4	32	<2	68
7	12	2.7	5.4	5.4	32	<2	65
8	11	5.0	5.4	5.4	33	3.0	68
9	8.9	4.0	5.6	5.6	33	2.4	67
10	7.1	9.0	5.7	5.7	26	5.5	61
11	6.0	4.5	5.6	5.6	26	5.9	57
12	6.6	2.3	5.7	5.7	23	<2	54
13	9.0	2.9	5.7	5.7	35	<2	65
14	9.7	2.2	5.1	5.1	37	<2	63

Table 3. Process sequence for SC1 treatment

Sulfuric Chemistry	Acid Treatment Time, min	Post SPM Rinse	SC1 Chemistry	Post SC1 rinse	Rinse/Dry	Temp °C
SPM (6:1)	10	QDR	1:2:100	QDR	IPA-Green Dry	50

Table 4. Anion and Cation Residues on the wafer surface following SPM followed by SC1 rinse

Test Run #	Anions, 10^{11}(x atoms/cm^2)					Cations (x 10^{11}atoms/cm^2)	
	F^-	Cl^-	NO_2^-	NO_3^-	SO_4^{-2}	Na^+	NH_4^+
Control	3.1	12	<2.0	8.3	<1.0	4.9	48.0
1	<2.5	15	11	10	1.9	<2.0	41.1

Table 5: Average particle (>0.16 μm) adders on the wafer for various OFR times following SPM and SC1 cleans. The QDR time is kept constant.

Process	OFR Time, min.	Average Particle (>0.16 μm) adders (post-pre)
SPM+ QDR + SC1 + QDR + OFR	2	19.6
SPM+ QDR + SC1 + QDR + OFR	4	-10.6
SPM+ QDR + SC1 + QDR + OFR	12	-32.4
SPM+ QDR + SC1 + QDR + OFR	14	-14

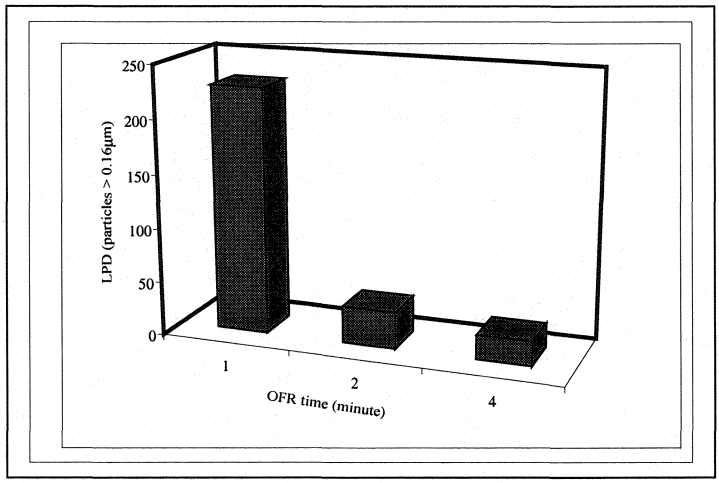

Figure 1. LPD Growth after 31 hours in class-10 clean room vs OFR at constant QDR of 5.5 minutes following SPM treatment of wafer.

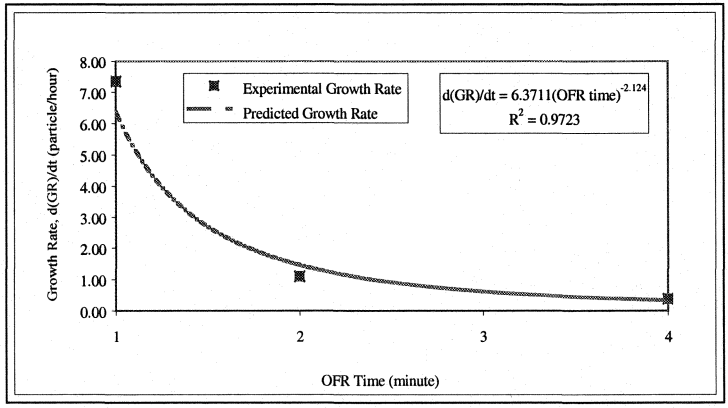

Figure 2. Growth rate of contaminants in class-10 clean room (after an SPM clean) as a function of OFR time.

PARTICLES

SUB 100NM PARTICLE REMOVAL WITH DEIONIZED WATER AND A MEGASONIC FREQUENCY OF ~835KHZ

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Theoretical and experimental investigations have demonstrated the ability of a single wafer megasonic cleaning system to remove particles less than 100nm in size from a wafer surface. The acoustic streaming forces created at the particle-wafer interface are the primary forces considered for particle removal. These forces are large enough to overcome the Van der Waals adhesion force for particle sizes less than 100nm. Experimentally, the Verteq Goldfinger single wafer megasonic cleaning system removed particles from O_3 last wafer surface using only room temperature de-ionized water and a megasonic frequency of ~835kHz. The particle sizes removed with this cleaning system include 80 ± 9nm SiO_2, 60 ± 3nm PSL and 36 ± 10nm SiO_2. Cleaning efficiencies ranged from a low of 97 ± 1% for the 36 ± 10nm SiO_2 and a high of 99.994 ± 0.002% 80 ± 9nm SiO_2 for a sixty-second megasonic cleaning time.

INTRODUCTION

It is well known that as device dimensions shrink, so will the size of the defect that need to be removed from the wafer surface to prevent device failure. A common cleaning technique to remove particles involves megasonic agitation during the cleaning cycle [1]. Particle sizes down to 100nm have commonly been removed by megasonics even though theoretical papers on megasonics (frequency ~ 1MHz) indicate removal of particles this small should not be possible [2]. It is believed that the dominant mechanisms of particle removal in megasonic cleaning include cavitation, microstreaming, and Schlichting streaming. By controlling the combination of these factors, finer particle removal could be realized in megasonic cleaning. Theoretical models and calculations which consider these mechanisms have been developed to predict removal rates of particles from silicon wafers, even below 100nm in particle size [3]. The purpose of this paper is to provide a theoretical explanation of megasonic particle removal and direct experimental evidence that megasonics is indeed capable of removing particles below 100nm.

The exact mechanism behind the megasonic removal of particles from wafer surfaces is still under investigation. Continued progress has been made to better understand the physical forces involved in removing particles with acoustic agitation. Various theories have been proposed in the past with claims to a fundamental size barrier to particle removal. A limiting factor to these claims has been the absence of experimental evidence within the same work to confirm or deny the existence of a fundamental size barrier. This paper will not only provide an up to date theoretical explanation of particle removal but also provide experimental evidence to confirm the theory. The main conclusion to result from this work is the absence of any fundamental size barrier to particle removal using acoustic forces.

Megasonic cleaning has been widely used in semiconductor wafer manufacturing for many years. The mechanism of fine particle removal has also been investigated for equally as long. Figure 1 shows a comparison between Van der Waals force to various removal forces for a PSL particle based on a few investigators' models [4]. According to Figure 1, megasonic cleaning can not remove fine particles.

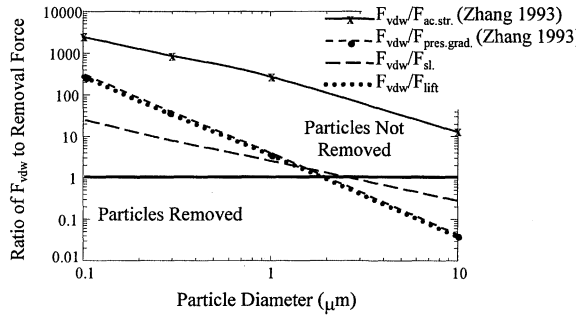

Figure 1. PSL particle removal by sliding and lift forces and by forces due to pressure gradient and acoustic streaming in the bulk region. Plotted are the ratios of adhesion Van der Waals forces to removal forces as a function of a particle size (PA = 3 atm, f = 850 kHz, cited from (4))

However, in practice, megasonic cleaning can easily remove submicron PSL and Si_3N_4 particles as well as slurry particles from silicon wafer surfaces. The reason why the models in Figure 1 have conflicts with real tests is that these models only consider liquid flow behaviors in the bulk region under a megasonic field. In megasonic cleaning, a silicon wafer surface has a very thin boundary layer called the acoustic boundary layer. Within this boundary layer (~0.60 μm at 1MHz) fluid motion with vortices (Schlichting streaming) and many micron size bubbles are generated (microstreaming and cavitation) which contribute significantly to particle removal. The theory presented in this paper will include the particle removal effects within the acoustic boundary layer.

To experimentally verify the theory, wafers were contaminated with slurry sizes below 100nm and cleaned with a Verteq Goldfinger™ single wafer megasonic [5-7]

shown in Figure 2. The transducer was operated at ~835kHz delivering ~ 0.04 W/mm^2 to the wafer surface.

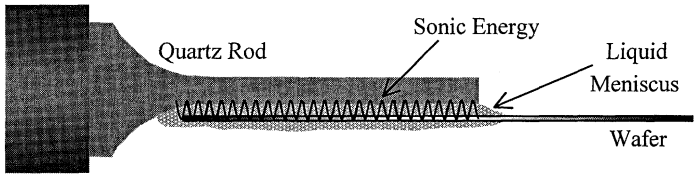

Figure 2: Cross sectional view of a Verteq Goldfinger™ Single Wafer Megasonic Cleaner. The wafer is held horizontally and rotated below the quartz megasonic transducer while liquid is applied to the top and bottom of the rotating wafer surface. The megasonic energy is transferred from the quartz rod to the wafer through the liquid meniscus.

The metrology to measure particle sizes below 100nm is possible with the KLA Tencor SP1-TBI. Particle sizes down to 60 nm can be measured using conventional LPD bin sizes while LPD sizes below 60 nm can be detected with the average haze channel. Both the LPDs and haze are detected with the dark field wide oblique (DWO) channel in this work [8,9].

EXPERIMENTAL

Both SiO_2 and polystyrene latex (PSL) particles were investigated to verify the megasonic removal theory. The 36 ± 10nm and 80 ± 9nm particles were SiO_2 and the 60 ± 3nm particle was composed of PSL. All particles were deposited on O_3 last silicon wafers (0.6 – 1 nm thick oxide) and were cleaned before contamination with a hydrophilic IMEC clean.

The particle contamination procedure consisted of a slurry bath at low pH containing the desired particles. Wafers were dipped in the particle bath, rinsed and then Marangoni dried. The contaminated wafers were then analyzed on the KLA Tencor SP1-TBI before megasonic cleaning. Typically, the particles were allowed to dry on the wafer surface after contamination to increase the adhesion force of the particles to the wafer surface. Particle removal efficiencies were then determined after a sixty-second megasonic clean, five-second rinse and Sahara surface tension gradient dry [10].

The particle removal is quantified by the percent of LPDs removed as determined by equation [1]:

$$\%\ \text{LPD Removal} = \frac{(\text{LPD added by contamination} - \text{LPD after megasonic clean})}{(\text{LPD added by contamination} - \text{LPD before contamination})} x\,100 \quad [1]$$

For the 36 ± 10nm SiO_2 particle, the average haze was used to determine removal efficiency [9]. In this case, equation [1] is modified to monitor the change in average haze instead of LPD removal on the wafer surface. Additionally, for the 80 ± 9nm and 60 ± 3nm particles the amount of LPDs on the wafer surface before and after the clean will be reported. The inclusion of this quantity will give a better understanding of the cleanliness of the wafer surface after the megasonic clean.

It should also be noted that no chemistry or heating was used during the megasonic cleaning, rinsing or drying of the wafers in any of these experiments. The megasonic transducer was operated at ~835 kHz and delivered ~ 0.04 W/mm^2 to the wafer surface.

RESULTS

Theory for Small (<100nm) Particle Removal by Megasonics

In megasonic cleaning, a silicon wafer surface has a very thin boundary layer called the acoustic boundary layer [11]. The thickness of this layer is proportional to the square root of the ratio of fluid dynamic viscosity to the frequency of the sound (about 0.6μm at 1 MHz). In this layer, the fluid is compressible and rotational so that the Reynolds stress is very large and many vortices occur. The scales of these vortices are determined by the thickness of the boundary layer, and their dimensions are much smaller than the sound wave length. The fluid motion with vortices in this boundary layer is called Schlichting streaming. In general, due to these vortices in the acoustic boundary layers, the velocity gradients of Schlichting streaming are much higher than the flow in the bulk region. In addition, many micron size bubbles are generated adjacent to deposited particles in this acoustic boundary layer, which results in microstreaming and cavitation.

The dominant mechanism of particle removal in megasonic cleaning results from the Schlichting streaming, the microstreaming, and the cavitation. Due to acoustic boundary layers and large Reynolds stress, streaming driving body forces (the source terms in the Navier-Stokes equation) in the local region of the particles deposited on

wafer surfaces are very large. Using Nyborg's theory [12], increasing power and frequency are effective ways to increase this kind of driving body forces in the acoustic boundary layer. These force gradients in an acoustic boundary layer in DI water for the power of 250 watts at the frequency of 850 kHz will be about 2.8×10^9 dyne/cm^4. For the power of 5 watts at the frequency of 3.4 MHz, the force gradients will be about 2×10^{10} dyne/cm^4 [13]. The subsequent Schlichting streaming velocity gradients in the layers also are very large, which result in strong drag forces. The drag force (F_{drag}) can be estimated using Stokes law as in Equation [2]:

$$F_{drag}=3\pi\mu dpV_{ave} \qquad [2]$$

Where μ is dynamic viscosity of the medium (0.01 g/cm-s for water)
dp is the diameter of the particles (cm)
V_{ave} is the averaged flow velocity in the acoustic boundary layer (cm/s).

For the particles of 0.1 μm in diameter, if the Schlichting streaming velocity exceeds 25 cm/s, the ratio of the adhesion force to the removal force (only the drag force) will be less than 1 [14]. A ratio less than one indicates particle removal. It is possible to increase V_{ave} of Schlichting streaming in acoustic boundary layers up to reasonable values using higher megasonic frequency. However, simply increasing megasonic frequency will bring a negative impact by reducing microstreaming and cavitation.

Microstreaming and cavitation in megasonic cleaning depend upon many factors. These factors include acoustic pressure, frequency, liquid viscosity, liquid surface tension, heat conductivity, contents and size of the nuclei, for example. For small nuclei of less than 0.5μm in diameter, surface tension effects are dominant for bubble motion and cavitation threshold. For large nuclei, the inertial and viscous effects are dominant. Bubble formation actually is a process of nucleation under negative sound pressure cycles. On the other hand, once the bubbles are generated from nucleation in a megasonic field, these bubbles will undergo a pulsating motion causing microstreaming to occur around these bubbles. Microstreaming continues to bring fresh air dissolved in the water or water vapor in the local region of these bubble surfaces. This speeds up rectified diffusion, which involves gas from the liquid diffusing into the bubble [15]. Rectify diffusion and megasonic pulsating motion result in a bubble growing. Once the bubble surface tensions can not undergo megasonic pressure in a positive sound cycle, the bubble will collapse causing cavitation.

In general, the scale of microstreaming velocity due to the pulsating bubble motion is above an order of magnitude greater than Schlichting streaming. Microstreaming is generated in a dynamic acoustic-moving-boundary layer by the pulsating bubble. At the moment of bubble collapse, the scale of microstreaming is

around one hundred meters per second due to shock wave generation. Rayleigh inferred the bubble collapsing time (τ) given by equation [3].

$$\tau \approx 0.915 R_{max}(\rho / P_o)^{0.5} \qquad [3]$$

Where R_{max} is the maximum radius of a bubble before collapse
ρ is air density
P_o is pressure.

For a bubble with a micron diameter under one atmosphere at 20°C, the bubble collapsing speed is 345 m/sec. Since acoustic pressure in megasonic cleaning is higher than one atmosphere, the bubble collapsing speed should actually be higher than the value above. Therefore, based on the description above and Equation [3], the ratio of the Van der Waals force to the drag force generated by microstreaming for a 0.1 μm PSL particle is lower than 0.25 during the bubble pulsating period and lower than 0.00068 during the bubble collapsing.

Acoustic cavitation has two important characteristics. First is its non-linear property between bubble radius and sound pressure. Second is that the potential energy installed in bubbles can be accumulated by abstracting sound energy [3]. When the bubbles collapse, this energy transfers into kinetic energy and is concentrated in a very tiny volume. This process causes very high pressures and temperatures (1,000 K) resulting in sonoluminescence which can be detected using a photomultiplier tube. Also, this process initiates or speeds up some chemical reaction.

It is possible to obtain several thousands atmospheres of pressure in a collapsed bubble region from cavitation in megasonic cleaning. In general, due to extremely high pressures, temperatures, shock waves, and microstreaming (generated from bubble cavitation) megasonic cleaning is able to remove fine particles with sizes below 0.1 μm. Along with these forces, there is danger for megasonic bubble cavitation to destroy fine structures on patterned wafers. Increasing frequency is an effective way to reduce cavitation as well as pattern damage with a price of reducing the cleaning efficiency. According to Holland and Apfels' theory [16], if acoustic frequency increases from 1 MHz to 4 MHz, the cavitation thresholds will increase from 7 atm to 9.2 atm for the nuclei radii of 0.1 μm. Theoretically if higher frequency is used in megasonic cleaning for removing particles smaller than 0.1 μm in diameter, the corresponding power inputs for the megasonic transducer should be increased to generate cavitation bubbles due to higher cavitation thresholds. It is not too difficult to run a cleaning process to remove fine particles at frequencies up to 5 MHz provided that the megasonic transducer is specially designed and acoustic power, chemical components, and temperature are well controlled.

It is possible to decrease cavitation thresholds at lower frequencies by increasing the temperature of the liquid medium or by changing the liquid viscosity by controlling the chemical components in the liquid medium. These methods are actually used for bubble size and density control in megasonic cleaning.

Experimental Results: Removal of Small Particles (<100nm) by Megasonics

The data to confirm the megasonic removal of small particles is presented below. Table I contains the particle or haze levels for the 80 ± 9nm SiO_2, the 60 ± 3nm PSL, and the 36 ± 10nm SiO_2 particles added to an O_3 last silicon wafer.

Table I: The particle levels before contamination, after contamination, and after a single wafer megasonic clean with de-ionized water. The 80 ± 9nm and the 60 ± 3nm particles were measured with LPD bin sizes and the 36 ± 10nm particles were measured with the average haze.

Particle Size	KLA SP1 TBI DWO	Before	With Contamination	After Megasonic Clean
80 ± 9nm	60nm<ϕ_{LSE}<120nm	2899±111	~3 x 10^6	3062 ± 68
60 ± 3nm	60nm<ϕ_{LSE}<120nm	2956 ± 67	~96,000	3584 ± 89
36 ± 10nm	Average Haze (ppm)	0.025 ± 0.001	0.25ppm	0.033 ± 0.003

The lower LPD size limit of the KLA Tencor SP1-TBI is 60nm. Monitoring the average haze on the wafer surface can lower the size range even farther. As contamination is added to the wafer surface, the average haze will change in response to the change in surface roughness. Typically, a large number of particles are required to change the average haze significantly enough for analysis. In the 36 ± 10nm SiO_2 case, ~3 x 10^{10} particles are added to the wafer surface during the contamination procedure [8].

The particle removal efficiencies for each particle size cleaned off of the wafer surface is shown in figure 3. Extending the cleaning time for the smallest sized particles results in complete removal of the 36 ± 10nm particles. The average haze values were returned to the original starting level with the additional cleaning time (100 ± 1% removal efficiency).

Clearly, the single wafer megasonics used in these cleaning studies is capable of removing nano-particle contamination in agreement with the proposed theory.

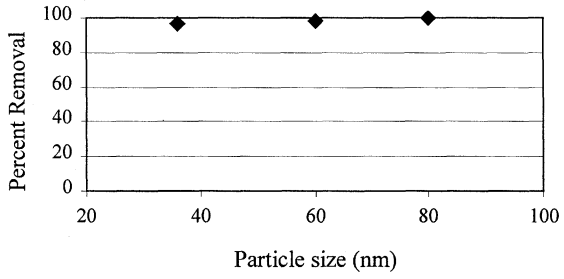

Figure 3: Removal efficiencies of 80 ± 9nm SiO_2 particles 60 ± 3nm PSL and 36 ± 10nm SiO_2 calculated from the data listed in Table 1. The removal efficiencies are 99.994 ± 0.002% for the 80 ± 9nm SiO_2 particles, 98.6 ± 0.2% for the 60 ± 3nm PSL, and 97 ± 1% for the 36 ± 10nm SiO_2 particles.

CONCLUSIONS

The current theoretical explanation examines different forms of acoustic streaming caused by megasonic agitation. The most important form of acoustic streaming for sub-micron particle removal is microstreaming caused by cavitation. These forces occur at the particle-wafer interface. Accounting for these forces clearly shows megasonics can provide the removal force necessary to clean sub-100nm particles from the wafer surface. Only accounting for bulk effects will result in an inaccurate estimation of megasonic particle removal ability.

The verification of the theory was provided experimentally with the Verteq Goldfinger single wafer megasonic system discussed in this work. All particle sizes examined (36 ± 10nm SiO_2, 60 ± 3nm PSL, and 80 ± 9nm SiO_2) were cleaned off of the wafer surface using a megasonic frequency of ~835 kHz and a power level of ~0.04W/mm^2 with only room temperature, de-ionized water. The LPD and average haze measurements clearly proves megasonics can removes nano-particle sizes efficiently and effectively.

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EFFECTS OF H_2O_2 AND IPA ADDITION IN DILUTE HF SOLUTION ON SURFACE ETCHING AND PARTICLE REMOVAL EFFICIENCY

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The purpose of this study was to evaluate the etch mechanism and particle removal efficiency in dilute HF solutions added with H_2O_2 and IPA. The etch rate of SiO_2 in HF solution was dependent on the etching time and concentrations of HF. As the concentration of H_2O_2 increased, the etch rate of SiO_2 increased. However, the etch rate of SiO_2 decreased as the concentration of IPA in HF solution increased. The etch rate of SiO_2 in HF-H_2O_2-IPA solution was very similar to that in HF-IPA solutions. The etch rate was dominantly dependent on IPA concentration not on H_2O_2. No significant difference in etch rate of silicon was observed in HF solutions with and without the addition of IPA. However, the etch rate of silicon increased in HF solution with the addition of H_2O_2. Higher contact angles were observed in the presence of IPA in HF solution. It might be due to the prevention of surface re-oxidation by IPA in HF solutions. Particle removal over 90% was achieved when Si wafers were cleaned in HF-H_2O_2 and HF-H_2O_2-IPA solutions.

INTRODUCTION

The dilute HF last cleaning has been widely used for the removal of native or chemical oxide on silicon wafer surface grown during wet treatment, especially before gate oxide growth because the reliability of oxide is degraded by the presence of native oxide [1]. As the thickness of gate oxide decreased to about several angstroms, however, the generation of micro-roughness [2] and particle contamination [3] and formation of water mark [4] during DHF step have been risen issues. Also it was reported that severe metal species, especially copper, contamination occur during DHF treatment by several authors [5-7]. All of these defects and contaminants are detrimental to the reliability of device characteristics and result in the failure of device. Thus, it is essential to reduce the contamination and monitor the state of the silicon surface and thin films at an atomic level by using proper cleaning chemistry that render the surface inert and leave an atomically flat surface after the cleaning process.

HF last cleaning can remove the native oxide and metallic contamination included in oxide. However, this step cannot remove the noble metal, such as Cu and Au, because the noble metals contaminated on Si surface electrochemically. It was proposed [8] that the addition of H_2O_2 in HF can remove the noble metal due to high oxidizing power of H_2O_2. However, the micro-roughness of Si surface can be increased in HF-H_2O_2 solutions because of local oxidation of Si surface and metal impurities [9].

In recent days, various methods have been proposed and examined to prevent these problems as mentioned above. The addition of surfactant or alcohol in dilute HF solution was effective for decreasing the surface micro-roughness [7, 8] and reducing the particle contamination [9]. It is very important to study the etch behavior of silicon dioxide and silicon wafer in dilute HF solution mixed with the additives, such as IPA and H_2O_2 for the process development. However, it has not yet completely understood the chemistry of HF solution with additives.

In this paper, we report the effect of the addition of isopropyl alcohol (IPA) and H_2O_2 on etch dynamics of silicon dioxide and silicon wafer. The surface was characterized by AFM and contact angle after the treatment in various HF solutions. The removal efficiency of particles was evaluated in various HF solutions with and without the addition of H_2O_2 and IPA.

EXPERIMENTAL MATERIALS AND PROCEDURES

In this study, 8" p-type (100) silicon wafers (resistivity : 3~11 Ω• cm) and silicon dioxide wafers (thermally grown oxide, ~ 4000 Å) were cut into 13 mm × 19 mm. Both types of wafers were cleaned in a 4:1 mixture of H_2SO_4 and H_2O_2 for 10 min and followed by 0.5% HF dipping in order to remove native oxide layer on wafer surface. The semiconductor fabrication grade chemicals, NH_4OH (28 wt% NH_3), H_2SO_4 (98 wt%), IPA (99 wt %) and H_2O_2 (32 wt%) were provided by Dong-Woo Fine Chem., used for the experiments. HF (49 wt%) was provided by Hashimoto chemicals.

The etch rates of silicon wafers in cleaning solutions were measured by analyzing the silicon concentrations in the solutions using an Inductively Coupled Plasma Mass Spectrometer (ICP-MS). The silicon wafers were immersed in 100 ml of various HF solutions for 1hr. The etch rates of silicon dioxide were measured by a Nanospec AFT 200 of Nanometrics. The HF solutions with IPA and H_2O_2 were stirred for 20 min before the experiments to make sure the homogeneous mixture. The contact angle was measured using Krüss G10 drop shape analyzer as functions of HF treatment time and DI water rinsing time.

Alumina (50 nm in diameter) and SiO_2 (14 nm) particles purchased from Deggusa and Beulher were used for the particle removal test and particles were contaminated on

silicon surface using the aerosol method. The particle removal efficiency was evaluated by a Surfscan (Tencor 5500) in various HF solutions.

RESULTS AND DISCUSSIONS

Even though the removal of silicon dioxide films via dissolution in aqueous HF solution is a key process step in practically all silicon-based micro-fabrication technologies, the etch mechanism of SiO_2 in HF solution are still disputed.

The following reactions have been generally accepted to be the chemical reactions of HF for the etching of SiO_2 [10].

$$HF = H^+ + F^- \qquad k_1 = 0.0013 \qquad (1)$$

$$HF + F^- = HF_2^- \qquad k_2 = 0.104 \qquad (2)$$

The dissociation constant of HF (k_1) is larger than formation constant of HF_2^- (k_2). So, the k1 determined an overall reaction. HF and HF_2^- concentrations were the important species to decide the etch rate of SiO_2 in HF solution. In these reactions, HF_2^- concentration plays an important role in controlling the etch rate of SiO_2.

Figure 1 (a) shows the etched SiO_2 thickness as a function of etch time at various HF concentrations. The etched thickness of SiO_2 linearly increased as the etching time increased. Figure 1 (b) shows the etch rate of SiO_2 as a function of etch time. For 30 second, the etched thickness was 20 Å and the etch rate was about 40 Å/min. As the etch time was increased, the etch rate was decreased drastically and then reached a constant rate of 23 Å. The high etch rate at the initial stage of etching mighty be due to a faster diffusion of etching species. According to the etch reaction described above, reaction (1) is thought to be the rate limiting reaction, because it requires diffusion of HF molecules onto reaction surface [11].

Figure 2 shows the etch rate of SiO_2 as a function of H_2O_2 concentration in 0.5 wt% HF solutions. The etched thickness of SiO_2 also linearly increased as the etch time increased when H_2O_2 was added in HF solution. It was very interesting that the etch rate of SiO_2 in HF solution was increased from 23 Å/min to 31 Å/min when 20 wt% H_2O_2 was added. The mechanism of the increase of etch rate when hydrogen peroxide was added in HF solution is not still understood clearly. As shown in Figure 3, the addition of IPA to HF solutions decreased the etch rate of SiO_2. The etch rate was decreased from 23 Å/min to 10 Å/min as the IPA concentration increased to 30 wt% in HF. The decrease of etch rate was due to the decrease of HF dissociation constant by the addition of IPA [12].

In the case of HF-H_2O_2-IPA solution, the effect of H_2O_2 addition on etch rate of SiO_2 was negligible and the etch rates were very similar to those of HF solutions added with IPA. Figure 4 shows the etch rate of SiO_2 as a function of IPA concentrations when 5 and

10 wt% H_2O_2 were added in 0.5 wt% HF solutions. IPA should more dominant effect on HF etch rate of oxide than H_2O_2.

To study the effect of H_2O_2 and IPA addition in HF solution on the reaction with silicon wafer, etch rate of silicon wafer in HF solution was measured. As shown in Figure 5, no significant difference in etch rates was observed among HF solutions with and without the presence of IPA. The addition of H_2O_2, however, increased the etch rate of silicon. The increase of etch rate may be due to the two competitive reactions, surface oxidation by oxidizing agent, H_2O_2, and the etch of silicon oxide by HF. However, the addition of IPA in HF-H_2O_2 solution decreased the etch rate of silicon wafer down to ~0.5 Å/min which was almost the same etch rate as that in HF-IPA solution. It was very important result that the HF-H_2O_2-IPA solution can control the etch rate by mixing the proper concentration of IPA. The control of etch rate in cleaning solution is very important because the thickness of thin film is directly influence the device characteristic and the over etched surface often results in generation of surface roughness. Two theorems were reported to explain the decrease of etch rate as IPA was added in HF solution. It was reported that IPA reacted with hydrogen halides. As IPA react with HF, isopropyl fluoride was formed as by-products. Because F- ions were consumed with IPA, formation reaction of HF2- was decreased. Finally, the etch rate of SiO_2 was decreased as dissociation rate of HF and HF_2^- concentration was decreased [12]. Also, Ohmi reported that etch rate was dependent on the dielectric constant of solution. From the coulomb force, when relative dielectric constant decreased with IPA addition, attractive force between H^+ and F^- is strengthened and dissociation of HF decreases and then etch rate is decreased [13].

To study changes of wettability after the treatment of wafers in HF-H_2O_2-IPA solution, the static contact angle was measured. Contact angle has been known to be very sensitive to the surface hydrophobicity. It is well known that the silicon wafer, conditioned in HF, passivated by hydrogen and it has a contact angle about 75°. As shown in Figure 6, the contact angle of silicon wafer that conditioned in HF-H_2O_2 solution was 73° without DI water rinsing. This contact angle was slightly lower than that of silicon wafer conditioned in HF solution. It might be attributed to a higher oxygen concentration in H_2O_2 containing HF solutions that in HF only. When the IPA added in HF solution, the contact angle increased to 83°. When wafer was treated in the case of HF-H_2O_2-IPA mixture, the contact angle was measured to be ~77° and higher than that in HF-H_2O_2 solution. This result indicates that the surface re-oxidation is prevented by IPA addition. This enhancement of contact angle is very important because it might represent the perfect hydrogen passivated Si surface and less residual oxygen on surface. The native and chemical oxide could give detrimental effect on thin gate oxide integrity [14].

The hydrogen passivated Si surface is stable against oxidation in air or in water [15], but the back bond of Si-H_x, Si-Si, is attacked and broken by oxygen. This oxygen forms a

SiO_x bond on silicon wafer surface. As this reaction is processed, the contact angle is decreased and wafer surface looses its hydrophobicity.

Figure 7 shows the changes of contact angle as a function of rinsing time after the treatment in HF, HF-H_2O_2, and HF-IPA solutions. The samples, conditioned in HF-IPA, show slightly higher contact angle than that in HF and HF-H_2O_2 solutions. After 60 minutes rinsing, the contact angle conditioned in HF-IPA solution was ~70°. This contact angle is higher than that of HF conditioned silicon wafer. Based on these results, it could be said that the silicon wafer, treated in HF-IPA solution, has more stable hydrogen passivated surface than the wafer treated in HF solution. The silicon wafer, treated in HF-H_2O_2, showed a relatively low contact angle.

Figure 8 shows the particle removal efficiency on wafers in HF-H_2O_2 and HF-H_2O_2-IPA solutions. SiO_2 and Al_2O_3 particles were intentionally contaminated on Si surface using aerosol method. Particle removal efficiencies over 90% were measured in both cleaning solutions. Because etch rate of SiO_2 was 25 Å/min in 0.5 wt% HF, it was expected that the SiO_2 (140 Å in diameter) particles might be dissolved in HF solutions. When the cleaning was performed for 10 min, the etch rate of SiO_2 was 250 Å/min. because we used to 140 Å silica particles in this study, the particles were almost dissolved in HF solution. It was assumed that particles were removed and etched at the same time in HF solutions.

SUMMARY AND CONCLUSIONS

The etch rate of SiO_2 in HF solution was dependent on the etching time and concentrations of HF and additives such as H_2O_2 and IPA. The etch rate of SiO_2 was changed as the dissociation of HF and concentration of HF_2^- were controlled by the addition of additives. The etch rate of SiO_2 in HF-H_2O_2-IPA was similar to that in HF-IPA solution. The etch rate was affected by the presence of IPA in HF-H_2O_2-IPA mixture. The effect of H_2O_2 on etch rate was minimal. No significant difference in etch rate of silicon was observed in HF solutions with and without the addition of IPA. However, the etch rate of silicon increased in HF solution with the addition of H_2O_2. When Si was treated in HF-H_2O_2-IPA, the contact angle was higher than that in HF-H_2O_2 solution. It indicates that the surface re-oxidation is prevented by IPA addition in HF solutions. And Micro-roughness of Si surface was dependent on the addition of H_2O_2 and IPA. Finally, HF-H_2O_2 and HF-H_2O_2-IPA solutions can remove the SiO_2 and Al_2O_3 particles effectively.

ACKNOWLEDGEMENT

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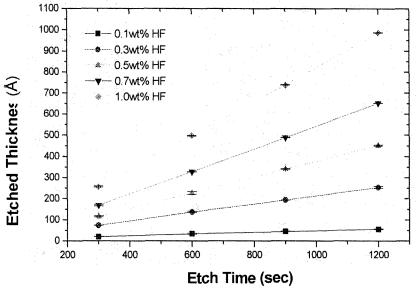
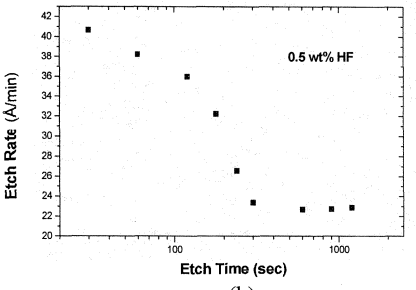


(a)



(b)

Figure 1. (a) The etched thickness of SiO_2 as a function of the HF concentrations and (b) the etch rate in HF solutions as a function of etch time

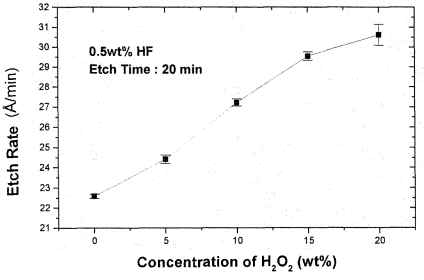


Figure 2. The etch rate of SiO_2 as a function of H_2O_2 concentration in 0.5 wt% HF solutions

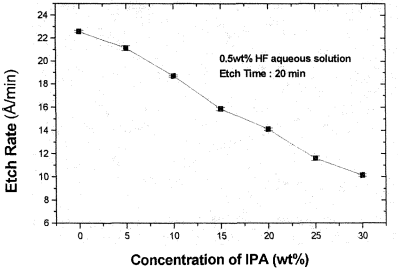


Figure 3. The etch rate of SiO_2 as a function of IPA concentration in 0.5 wt% HF solutions

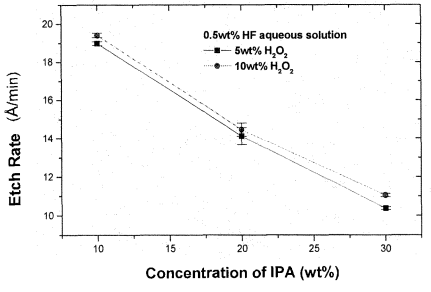


Figure 4. The etch rate of SiO_2 as a function of IPA concentrations at 5 and 10 wt% H_2O_2

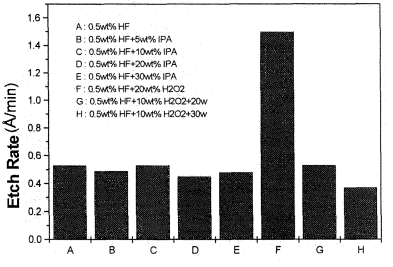


Figure 5. The etch rate of Si in various HF solution

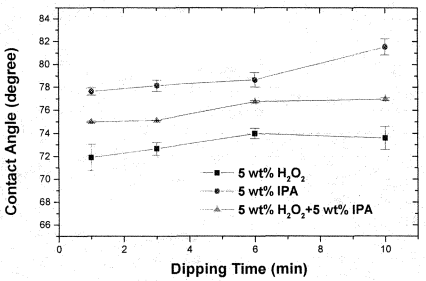


Figure 6. The change of contact angles as a function of dipping time in HF-H_2O_2, HF-IPA and HF-H_2O_2-IPA solutions

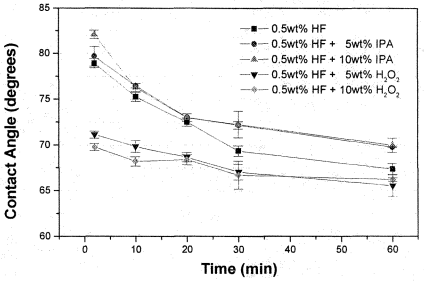


Figure 7. The changes of contact angle as a function of rinsing time when treated in HF, HF-H_2O_2 and HF-IPA.

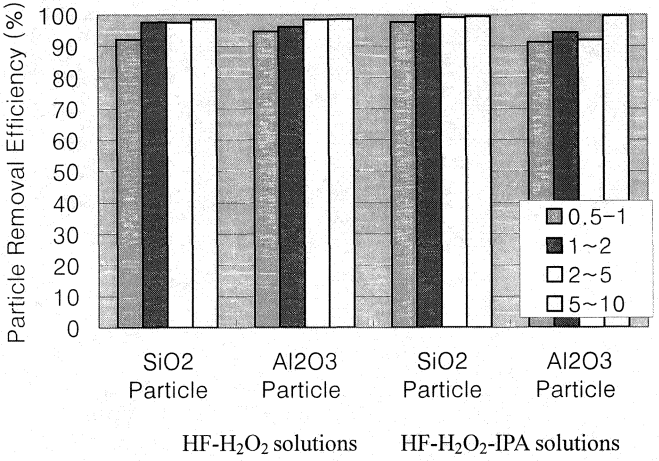


Figure 9. The particle removal efficiency in HF-H_2O_2 and HF-H_2O_2-IPA Solutions

ACTIVITY OF HF SOLUTIONS AND PARTICLE REMOVAL USING HF SOLUTIONS

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Removal of particles from silicon wafers by wet chemical processes generally involve etching the surface, and possibly the particle, by the cleaning chemical and the electrical potentials of the surface and the particle in solution (zeta potential). The etching of the materials and the zeta potential are themselves dependent on the pH, other ionic species present in solution and the ionic strength. This paper incorporates activity coefficients in the chemical calculations to model the pH and ionic strength of 1000:1 HF that has been spiked with HCl or NH_4OH. Experiments were performed to study the effect of pH, ionic strength, and etching on removal of SiO_2, Si, and Si_3N_4 particles from silicon wafers.

INTRODUCTION

HF solutions have been shown to be effective at removing particles from silicon wafers (1) due to slight etching of the native oxide on the wafer surface. Prevention of particle deposition onto silicon wafers in HF has been reported to be dependent on pH and ionic strength (2). Knotter and Dumesnil found that a solution pH > 2 resulted in lower particle deposition as long as the ionic strength was below about 0.5 moles/liter. This work investigates the converse, is the particle removal efficiency in HF solutions dependent on pH and ionic strength? Minimizing particle re-attachment during particle removal is necessary in order to have high particle removal efficiency. At least a small effect could be expected if any particles are removed from the surface in the first place.

In order to test the particle removal with an HF solution at different pH values we needed to know how to mix the solutions. The species in HF solution are H^+, HF, HF_2^-, F^-, and H_2F_2 (3) and the equilibrium constants for these species at 25 degrees Celsius are:

$$\gamma_{(H+)}[H^+]\gamma_{(F-)}[F^-]/[HF] = 6.85 \times 10^{-4} \quad [1]$$

$$\gamma_{(HF2-)}[HF_2^-]/[HF]\ \gamma_{(F-)}[F^-] = 3.963 \quad [2]$$

$$[H_2F_2]/[HF]^2 = 2.7 \quad [3]$$

Where γ denotes the activity coefficient for an ionic species. Using these equilibrium equations with charge balance and mass balance equations and assuming all the activity coefficients are unity, the concentration of each species can be calculated given the initial

amount of HF and other chemicals put into solution. Once the concentration of each species is known then the solution ionic strength, μ, is calculated using equation [4].

$$\mu = \frac{1}{2}\sum_i c_i z_i^2 \qquad [4]$$

Where c is the concentration of an ion in moles/liter and z is the charge of the ion. For low ionic strength solutions ($\mu < 0.001$), assuming activity coefficient are unity is reasonable. In our experiments where we have changed the pH of the solution by adding HCl or NH_4OH, the ionic strength of the solution is higher and including the activity coefficients becomes more important to calculating an accurate model of the solution. We have used the extended Debye-Huckel equation [5] to calculate ion activity coefficients.

$$\gamma = 10\text{^}\left(\frac{-0.512 z^2 \sqrt{\mu}}{1 + r\sqrt{\mu}/305}\right) \qquad [5]$$

Where z is the ion charge, and r is the hydrated radius of the ion. The hydrated radii used were 900 pm for H^+, 350 pm for F^-, and OH^-, 300 pm for HF^{2-} and CL^-, and 250 pm for $NH4^+$(4). Four iterations are made to refine the calculation of the activity coefficients and equilibrium equations until the solution converged.

From the constraining equations including activity coefficients we calculate the amount of buffer to mix with HF to get the desired pH at various species concentrations. We used a 1000:1 HF solution at various pH values to remove SiO_2, Si, and Si_3N_4 particles from Si substrates. The effect on the particle removal efficiency by the amount of oxide etched, pH, and ionic strength will be reported for each particle material.

EXPERIMENT

HF and pH adjustment chemicals were mixed to the ratios shown in Table I for the particle removal tests. Cleanroom grade 49% HF was used and volumes were measured in a Teflon volumetric flask. Cleanroom grade 37% HCl and 29% NH_4OH were used with these volumes being measured by burettes. The chemicals were placed into a 1 L volumetric flask and mixed with DI water. The resulting chemical mixture was placed into a chemical canister of a Mercury® spray processor system to be dispensed onto wafers after going through a 0.05 micron particle filter. The etching chemical was dispensed onto the wafers for 3 or 5 minutes at a flow rate of 2.0 liters/minute. Ozonated DI water (DIO_3) was dispensed onto the wafers for 3 minutes before the etching chemical to remove any organic contamination. DIO_3 was also dispensed onto the wafers for 5 minutes after the etching chemical to regrow a chemical oxide on the wafers and protect the wafers from particle contamination during the dry.

Table I: Chemical mixtures used in experiments

HF (ml)	HCl (ml)	NH_4OH (ml)	DI water (ml)	Mixture
1.0	10.1	0.0	988.9	1000:1 HF, pH 1
1.0	0.75	0.0	998.25	1000:1 HF, pH 2
1.0	0.0	0.0	999.0	1000:1 HF, pH 2.4
1.0	0.0	0.76	998.24	1000:1 HF, pH 3
1.0	0.0	1.71	997.29	1000:1 HF, pH 4

Wafers were contaminated with particles by preparing a slurry of particles suspended in a liquid and then dipping the wafers into it and spin drying the wafers leaving a controlled number of particles on the wafer surface. Approximately 2000 Si_3N_4 particles ≥0.12 μm size were deposited onto the wafers by preparing a slurry of 2 mg of dry Si_3N_4 particles in 100 ml of DI water and then diluting 87 μl of the particle slurry into 20 L of DI water and dipping the wafers for 2 minutes. Approximately 2000 Si particles ≥0.12 μm size were deposited onto the wafers by preparing a slurry of 60 mg of dry Si particles in 100 ml of DI water and then diluting 75 μl of the particle slurry into 20 L of DI water with 20 ml HCl and dipping the wafers for 4 minutes. Approximately 2000 SiO_2 particles ≥0.12 μm size were deposited onto the wafers by preparing a slurry of 45 mg of dry SiO_2 particles in 100 ml of DI water and then diluting 75 μl of the particle slurry into 20 L of DI water with 20 ml HCl and dipping the wafers for 3.5 minutes. For the Si and SiO_2 particles very low particle counts were achieved on the wafers in only DI water at pH 7, requiring the addition of a small amount of acid. Each particle type was contaminated onto the wafers in a dedicated tank and each tank was tested for particle cleanliness and was found to add less than 5 particles at >0.12 micron. Therefore, more than 99.75% of the particles added onto the wafers were made of the desired contamination material. The wafers were stored in a dry nitrogen environment for 15-20 hours before performing the particle removal tests.

Particles were measured on bare silicon wafers using a Tencor SP1-TBI inspection system using the oblique laser to illuminate the particles. The Tencor recipe placed the particles into bins of PSL sphere equivalent particles sizes 0.12μm – 0.16μm, 0.16μm – 0.2μm, 0.2μm – 0.25μm, 0.25μm – 0.3μm, 0.3μm – 0.5μm, and area counts larger than 0.5μm. Particles were measured on clean wafers before contamination (pre), the particles were measured after the wafers were contaminated (challenge), and the particles were measured after cleaning with the various processes (clean). The particle removal efficiency was calculated using equation 6. The particles added onto clean silicon wafers were measured for each cleaning process to ensure that the particle removal data was not affected by particle addition. In all cases very few particles were added onto the wafers and the contribution of particle addition on the particle removal efficiency was negligible.

$$\text{Efficiency} = 100 \times \left(\frac{(challenge - pre) - (clean - pre)}{(challenge - pre)} \right) \quad [6]$$

RESULTS AND DISCUSSION

Knowledge of the amount of chemicals to use to achieve a certain mixture is very important for a mixture of three chemicals because adjustments of the pH cannot be made after the mixture is prepared without affecting the concentration of HF and other species in solution. Figure 1 shows that for the more acidic mixtures inclusion of activity coefficients in the calculation of the chemical mixture is important. To make a pH 1 solution you should add 10.1 ml of HCl to make 1 L of solution if the calculation includes activity coefficients. If activity coefficients were not included in the calculation then one would naively add only 8.25 ml of HCl to make a 1 L solution. Because the pH is a log scale this difference in the amount of HCl would make a small difference in the pH of the solution. Figure 2 shows the concentration of species in solution calculated using our model for 1000:1 HF with the pH adjusted with HCl or NH_4OH.

Figure 3 shows the measured thermal oxide etch rate of the solutions used in the particle removal tests. Because the thermal oxide etch rate is very low some of the differences in the data could be attributed to noise in the oxide thickness measurement. Figure 3 also shows the calculated ionic strength of the solution in moles/liter. The ionic strength of the solution is lowest when no pH buffering chemicals are added to the 1000:1 HF. The ionic strength of these solutions are relatively low, except at pH 1, compared to the 0.1 – 0.5 moles/liter ionic strength solutions that are seen to affect particle addition onto wafers (2).

The effects on particle removal that we explored in our experiments are the amount of oxide etched, solution pH, and solution ionic strength. Our data for 1000:1 HF at pH 2 (HCl added) for three etch times, and for 1000:1 HF at pH 2.4 (no chemicals added) for two etch times, are plotted in figure 4 as the particle removal efficiency versus the amount of thermal oxide etched. It was assumed that if a 0 minutes etch process was performed that no particles would be removed. It appears that the particle removal depends on how much oxide is etched with very little particle removal occurring if less than 3 Angstroms of oxide is removed. This data supports the conclusion that the particles must be undercut and lifted off the surface before they can be removed.

It is apparent from figure 4 that Si_3N_4 particles are the most difficult to remove. This could be due to how hard the particles bond onto the wafer surface. Or it could be related to the fact that the particle removal solution is HF and this does not etch the Si_3N_4 particles while it will etch the SiO_2 particles and may perform some etching of the native oxide layer on the Si particles.

A clear trend in the data in figure 5 shows the effect on particle removal efficiency by changing the pH of the 1000:1 HF solution for a five minute etch time. However this trend in the pH data is not what we expected. We expected that the particle removal would improve as the solution pH became higher, just as the particle deposition becomes lower at higher pH values (2). Instead we found that the particle removal efficiency

peaked when no pH adjustment chemical was added to the 1000:1 HF. For all three particle types, when either HCl or NH_4OH was added to the 1000:1 HF, the particle removal efficiency decreased. The data point for Si_3N_4 particles at pH 3 was removed because for some unknown reason the particle removal efficiency was highly negative.

In order to change the pH of the 1000:1 HF solution, HCl or NH_4OH was added, which has the side effect of also changing the solution ionic strength as was shown in figure 3. Because of the confounding of pH and ionic strength figure 6 was made from the data with the arbitrary distinction between acidic and caustic chemicals added to the 1000:1 HF. Again the data point for Si_3N_4 particles at pH 3 was removed. Like figure 5, figure 6 shows that the particle removal efficiency peaks when no chemicals are added to the 1000:1 HF. For all three particle types, when either HCl or NH_4OH was added to the 1000:1 HF, the particle removal efficiency decreased. Additionally shown in figure 6 is data were the ionic strength of the 1000:1 HF solution is increased by adding a salt while not changing the pH of the solution. This data confirms that if the ionic strength of the solution is increased that the particle removal efficiency decreases.

The common property of the HF solutions with either HCl or NH_4OH added is that the ionic strength of the solution is increased when the chemicals are added and this has resulted in a decrease in the particle removal efficiency. The ionic strength is the main property of the solution that explains why the particle removal efficiency peaks when no chemicals are added to the HF and decreases when either a buffering acid or a caustic are added. It is interesting to note that the ionic strength of the solution affects the particle removal efficiency at lower values than it affects the particle addition. Where particle addition does not begin to occur until the ionic strength of a solution reaches 0.1 – 0.5 moles/liter (2), there does not appear to be such a threshold value for ionic strength on the affect of particle removal.

Figure 7 shows that for SiO_2 particles the larger particles are easier to remove from the wafers for all the tests that were performed. Figure 8 shows that for Si particles the larger particles are easier to remove from the wafers for all but one of the tests that were performed. Figure 9 shows that for Si_3N_4 particles the larger particles are easier to remove from the wafers for all the tests that were performed.

If increased ionic strength of the HF solution has the effect of reducing the particle removal efficiency, as shown above, then one way to improve the particle removal efficiency of HF solutions is to reduce the concentration of the HF. Figure 10 shows how the ionic strength of HF solutions is affected by dilution of the HF. Most HF etch steps are performed at concentration of 10:1 to 100:1. The ionic strength of these HF mixtures is fairly high and can be significantly reduced by going to concentrations of 500:1 to 1000:1 for steps were particle removal is a concern. If this is done then longer process times will be needed in order to etch enough oxide to remove the particles as the oxide etch rate is reduce when the concentration is lower.

CONCLUSIONS

We have found that several types of particles can be removed from silicon wafers with HF solutions with Si_3N_4 particles being the most difficult to remove. The more thermal oxide that is etched the higher the particle removal efficiency will be with several Angstroms or more needing to be etched. The particle removal efficiency was decreased if either HCl or NH_4OH was added to the 1000:1 HF. The reason for this is that the ionic strength of the solution is increased when these chemicals are added.

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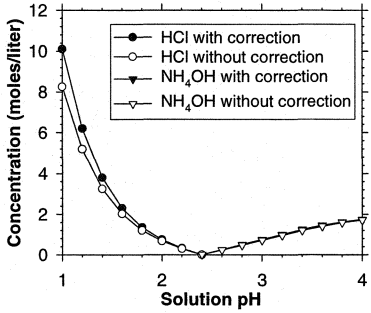

Figure 1: Volumes of HCl and NH_4OH added to shift the pH of 1000:1 HF solutions calculated with and without the inclusion of the effects of ionic strength.

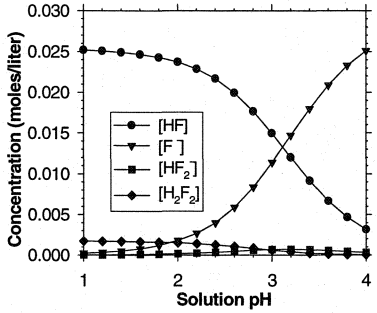

Figure 2: Calculated concentration of species of 1000:1 HF at different pH values.

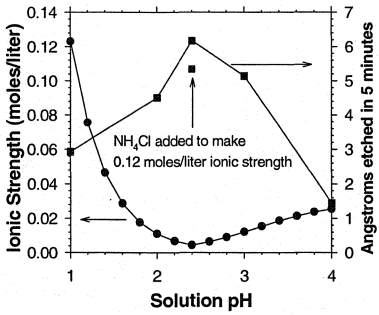

Figure 3: Ionic strength and etch rate of thermal SiO_2 in 1000:1 HF solutions spiked with HCl and NH_4OH to vary the pH.

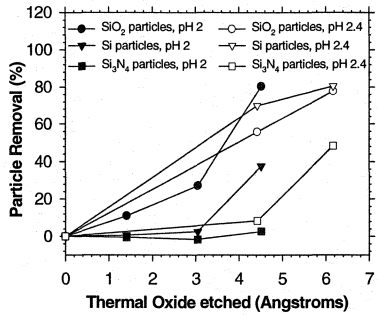

Figure 4: Particle removal as a function of the etch rate at pH 2, for 1, 3, and 5 minutes and no pH adjustment (pH 2.4) for 3, and 5 minutes.

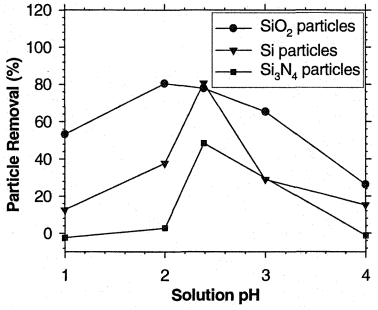

Figure 5: Particle removal as a function of pH.

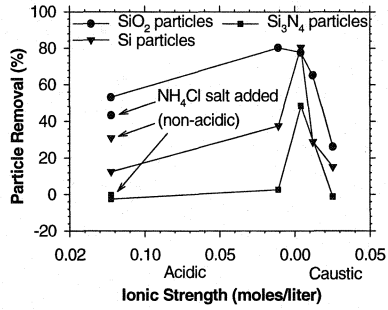

Figure 6: Particle removal as a function of ionic strength.

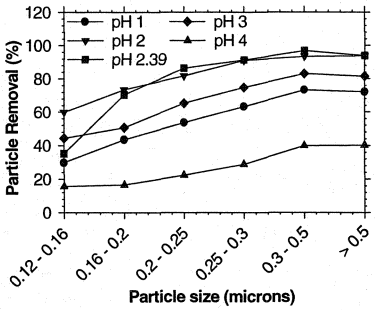

Figure 7: Removal of SiO_2 particles as a function of size and pH.

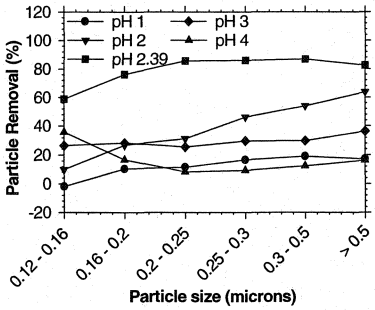

Figure 8: Removal of Si particles as a function of size and pH.

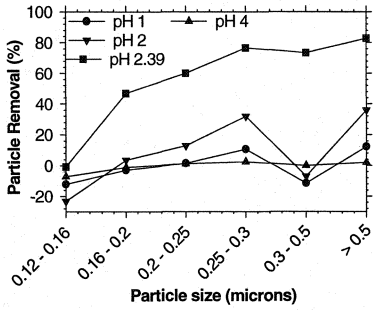

Figure 9: Removal of Si_3N_4 particles as a function of size and pH, excluding pH 3.

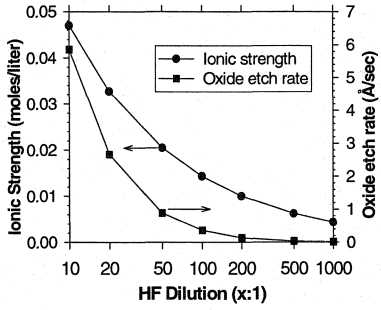

Figure 10: Solution ionic strength and calculated thermal oxide etch rate for dilutions of 49% HF.

EFFECT OF WAFER BACKSIDE ON PARTICLE ADDITION BEHAVIOUR OF HF-RCA SEQUENCE

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During the IC manufacturing process, some fabrication steps require an oxide removal before RCA cleaning. This etching step clearly appears to be very critical because any residual contamination left on the silicon surface can modify the critical oxide quality and affects the Q_{bd} results, on gate and tunnel oxides. Particle tests were carried out directly on production EPI wafers and showed an increase in contamination of 1000 particles at 0.15 μm per wafer. Most of the added particles were stuck at the bottom of the wafer and the RCA cleaning was not able to remove them. This paper summarises the results achieved in the study of HF steps and the wafers backside on particle contamination behaviour of HF-RCA and introduces the solutions found.

INTRODUCTION

The wafer cleaning process has been one of the most important and critical steps in semiconductor manufacturing for over 30 years since W. Kern and D. Poutien developed the well-know concept RCA cleaning in 1960 at RCA Laboratories [1]. Diluted HF chemistries (1 to 4%-*w*) are widely used for oxide etching on wafers, before critical gate oxidations, because of the high selectivity with silicon and the high etching rate that can be obtained with relatively low HF concentrations, at room temperature. Very often the SiO_2 removal step is integrated in the wet cleaning tool for surface preparation: wafers go through a diluted HF treatment followed by a RCA cleaning. This step is very critical, because any residual surface contamination can have a detrimental impact on the electrical device properties.

In many real manufacturing cases, when wafers are dipped in the HF bath for an oxide stripping sequence, it is possible to see a huge particle addition on both oxidised and bare silicon surface after the etching step (Figure 1). Previous investigations [2] carried out on conventional wet benches using multi-tank tool and re-circulated chemistries, showed that particle contamination is intrinsic to the HF etching in a recirculated bath and that the amount of contamination is tool or tank dependent. Moreover a major role is played by wafer backside status during the very first process steps. If the subsequent RCA cleaning is not efficient, severe gate oxide integrity (GOI) and device defectivity problems may arise.

In this paper the influence of HF steps and the wafer backside on the particle contamination behaviour of HF-RCA sequence will be investigated.

EXPERIMENTAL

All reported tests were carried out using a Dainippon Screen (DNS) FC821L. This tool features re-circulated tanks (CHB) and one-step, multi-chemistry modules (ONB). In ONB modules, as well as for other single tank tools, chemicals are not re-circulated but injected into a DIW flow. Therefore, only diluted chemistries, such as HF, NH_4OH, HCl, H_2O_2, can be used.

HF etching can be performed in both modules, while the rinse step and the following RCA cleaning are performed only in ONB modules. HF concentration was 1% wt in re-circulated tank or 0.3 % wt in ONB modules. SC1 mixing ratio was 1:2:100 at 50 °C.

This "hybrid tool" is able to load 50 wafers at half pitch face to face (polished side are opposite to the other polished side) or back to front configuration as well as 25 wafers at normal pitch (polished side opposite to the rear side of the previous wafer), as shown in Figure 2.

In order to study the effect of the backside surface, several kinds of prime wafers were used:

- epitaxially grown silicon with 3000 ± 1000 Å of LTO oxide on the back side and about 200 Å of thermal oxide on front side
- epitaxially grown silicon with 3000 ± 1000 Å of LTO oxide on the back side
- epitaxially grown silicon with 8000 ± 1000 Å of poly and 3000 ± 800 Å LTO oxide on the back side and about 200 Å of thermal oxide on front side
- epitaxially grown silicon with 8000 ± 1000 Å of poly on the back side

The experiments were performed loading three test wafers in the first three slots of the batch in full or half pitch configuration and then filling the remaining 22 slots with silicon dummies.

The measurement tool used for particle contamination is a KLA-Tencor SP1^{TBI}, measuring defects whose size is larger than 0.15µm or a KLA-Tencor AIT*II*. Edge exclusion was 5mm. Haze measurement was also carried out using the SP1^{TBI}. SEM analyses were performed on the Applied Material SEM Vision with an automatic review system. AFM measurements were made on a Park Scientific Autoprobe LS.

RESULTS AND DISCUSSION

The first test was performed loading 25 wafers, front to rear in full pitch. HF step was tuned to remove about 220Å of thermal oxide leaving a hydrophobic surface on wafer front side. Particle addition map is reported in Figure 1: the total number of defects was one hundred times higher than the typical defectivity-upper-control limit for a cleaning process. The amount of defects depends on the loading position, the first two wafers, which are facing an oxidised back-side, are heavily contaminated, while the third one, that faces the backside of a silicon dummy, is far less contaminated, even if not clean (see Figure 3). Further tests show that a certain contamination level is surprisingly found even if wafers are loaded front to front, at half pitch.

A possible explanation of the front side contamination mechanism has been reported in reference 2: it may be due to the different surface state of a hydrophobic (backside) and a hydrophilic wafer (front-side), since in these two states the meniscus formed during the wafer extraction from the HF bath is very different (Figure 4). Particles on the liquid surface move from the hydrophilic wafer to the hydrophobic one, with enough speed to win the repulsive force (Figure 5). The source of the particles can be either the wafer backside or the HF and DIW baths themselves.

In order to better understand the problem, bare epitaxially grown silicon wafers were processed using the same recipe and procedure. Total amount of added particles was about 200 at 0.15μm (see Figure 6). Similar results were obtained on another tool of the same model running 0.5 %-wt HF, and 40°C SC1 and on a tool from another manufacturer using a similar cleaning concept. On this tool the test were performed without the SC2 step, but with the same testing conditions (50 wafers loaded in half pitch, front side opposite to front side). Results reported in Figure 7 show a similar particle pattern, demonstrating that the problem is almost independent of the tool set-up.

At SEM review, the particles are different in shapes and sizes (see Figure 8), and the Auger analysis showed that the most relevant peaks are related to silicon and oxygen (see Figure 9). Furthermore AFM analysis reported in Figure 10 and Figure 11 did not show any roughness difference between the HF-RCA treated surface and the RCA one.

This kind of problem can be related to the previous one, considering the presence of an oxide layer on the EPI wafer backside. To verify this hypothesis, different wafer substrates were tested. Results are reported in Figure 12. For EPI wafers with an oxide layer on the backside the particle addition is very high, while for the ones with a single polysilicon layer there is no addition. Another experiment was performed removing the oxide from the wafer backside using a SEZ spin etcher, and performing the HF-RCA clean in the configuration described above. As illustrated in

Figure 13, AIT analysis did not show any anomalous defectivity.

Anyway, sometimes it is not possible to avoid or to remove the oxide from the wafer backside, without major changes to the process flow or device characteristics. In this case it is suitable to use a very effective SC1 process, with more concentrated chemistry and much higher megasonic energy or to add a surfactant to the HF bath as recommended in reference 2.

Alternatively it is possible to completely overcome all particle deposition issues by avoiding to cross the air/liquid interface and performing the etching and the cleaning step in the same tank. In this case a more diluted HF solution (0.3% wt) has been used, in order to keep reasonable chemical consumption.

In this case the particle deposition mechanism shown in Figure 4 cannot occur anymore because the liquid/air interface is crossed only after an oxidizing treatment (SC1), and hence when all wafers exhibits the same surface state, on both front and back sides. The drawback of this approach can be a longer process time, and a consequent lower equipment throughput.

Particle deposition of the single tank etch has been compared with the conventional approach in Figure 14. The latter does not show any particle addition after the HF-

RCA process, showing a very clean surface, with no hazing, roughening and pitting problems.

CONCLUSIONS

During the oxide layer etch in a HF tank, a large amount of the rear oxide is also removed, since the LTO oxide on the rear side of the wafer is etched in HF more rapidly than the thermal oxides on the front side. This creates a layer of floating particles in the solution. During the unloading step from the HF bath to the rinsing tank these particles stick on the hydrophobic wafer surface, for an electrostatic attraction mechanism.

These adhered particles can be removed by using a very effective SC1 step, with a high-energy megasonic treatment and a high concentration.

Since a strong SC1 is not always feasible, a different approach to the problem was needed. We have showed that removing the oxide from the wafer backside or performing the whole HF-RCA in the same tank can avoid this large particle adhesion.

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1 W.Kern and D. Poutien, RCA Rev 31,187 (1970)
2 E.Bellandi, M.Alessandri, F.Pipia and A. Tonti, Proc 4th Intl. Symp. UPCSS, Oostende, Belgium, 35 (1998)

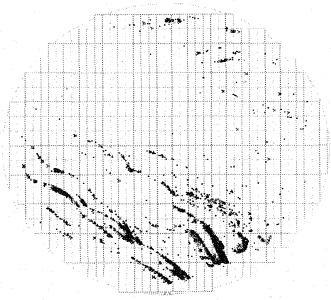

Figure 1: Particle contamination after HF strip observed at AIT II

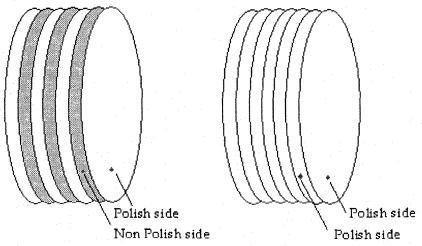

Figure 2: Wafer handling. Face to face (left) and face to back (right) loading.

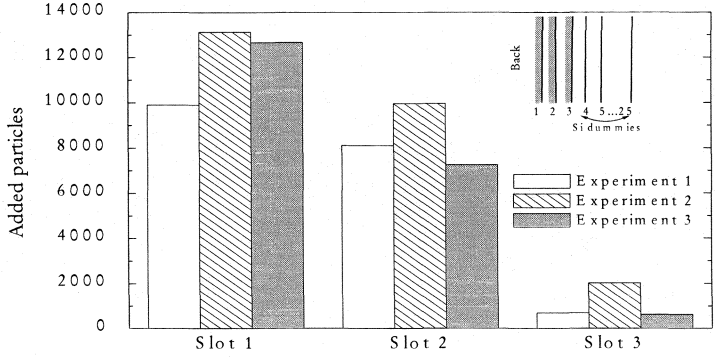

Figure 3: Particle count Vs wafer position

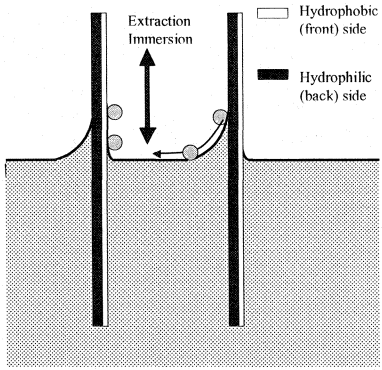

Figure 4: Mechanism of particle addition during wafer extraction

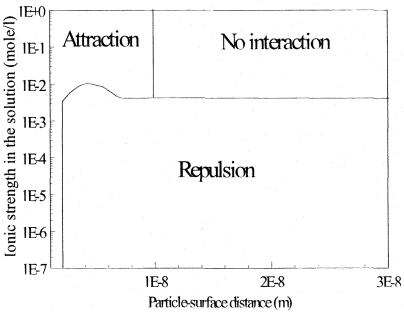

Figure 5: Simplified chart of particle to surface interaction (Z-potential is -10mV, wafer potential -300V)

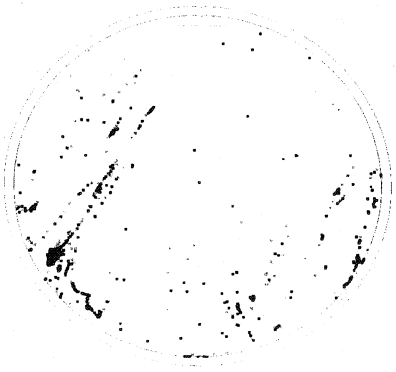

Figure 6: HF-RCA on a prime EPI wafer

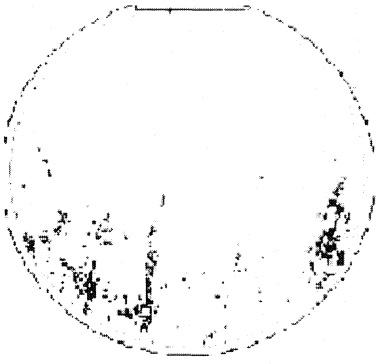

Figure 7: HF-SC1 on an oxidized EPI wafer performed on a tool from another brand.

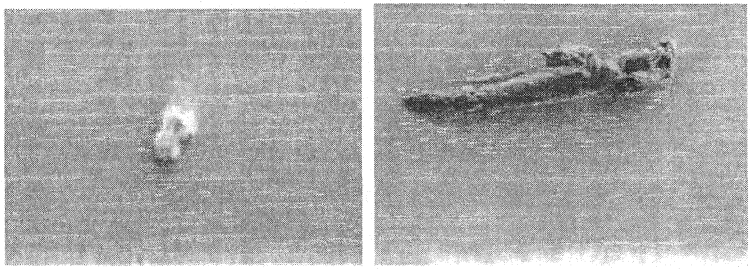

Figure 8: SEM image of the adhered particles

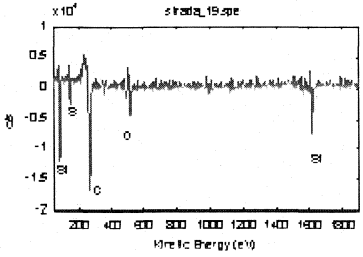

Figure 9: Auger analysis of the adhered particles, silicon and oxygen peaks are clearly evident

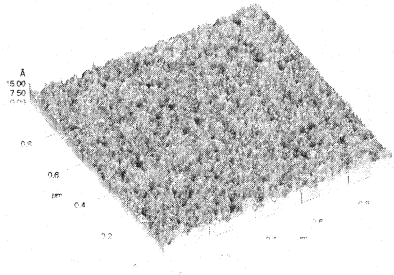

Figure 10: AFM analysis after HF-RCA clean

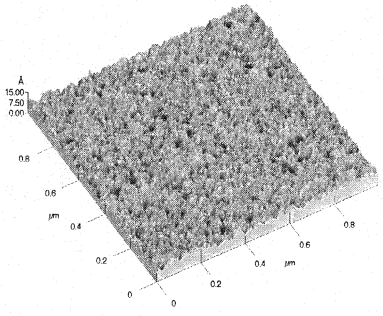

Figure 11: AFM analysis after RCA clean

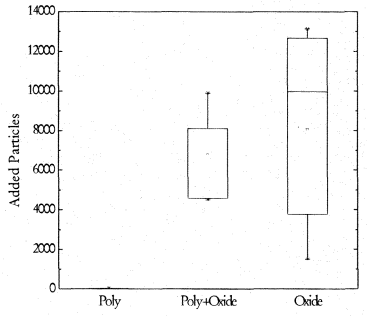

Figure 12: Particle count vs. wafer backside

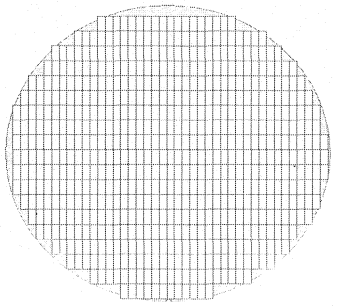

Figure 13: AIT analysis of a wafer whose rear oxide has been removed by an SEZ spin etcher

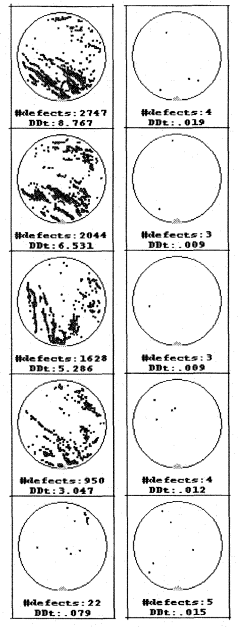

Figure 14 particles counts after recirculated HF (left) and single tank etch (right)

New Approach for Study of Particle Adhesion and Removal Relevant to Post CMP Cleaning

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The purpose of this study was to investigate the interaction force between slurry particles and wafer surfaces for the development of effective post Chemical Mechanical Planarization(CMP) cleaning process. Silica slurry has been most commonly used in the final step of Cu polishing to reduce scratches, Cu dishing and oxide erosion. The calculation and measurement of interaction forces between silica particles and TEOS, TaN and Cu surfaces have been performed in this study. DLVO theory was used to calculate the interaction force between the slurry particle and the wafer by measuring zeta potentials of particles and surfaces. The interaction force was directly obtained by measuring the force on the particles as a function of distance between the particle and surface using an Atomic Force Microscope. The strongest adhesion force was measured on TaN surfaces in both calculation and measurements. The magnitude of particles contamination on wafers was measured by FESEM after polishing. Highest number of particle observed on TaN surfaces after polishing.

INTRODUCTION

Due to its low resistivity and high electromigration performance, copper is considered to be a much better metallization than the currently used aluminum based alloys [1]. While the advantage of using Cu, as an alternative material to Al is clear, there are several challenges that must be overcome. One such challenge is the difficulty involved with Cu patterning by the dry etching (RIE). The damascene technology using Chemical Mechanical Planarization (CMP) is the only technology that can provide global planar surfaces and patterned copper with a large process window [2]. Other problem of Cu CMP is Cu contamination. Copper is considered as a very serious metallic contaminant for silicon devices. Also, detrimental effects of Cu contamination into the inter-metal and inter-level dielectrics were well known. Because Cu CMP give rise to many scratches, large dishing and easy erosion, two-step polishing has been applied in Cu CMP. In the first step, alumina slurry in acidic pH has been used for a faster removal of Cu until TaN surface just exposed. Alkaline silica slurry has been commonly used to meet the polishing selectivity of Cu : TaN : TEOS to 1 : 1 : 1.

After the 2nd step polishing, Cu, TaN and TEOS surfaces will be exposed to silica slurry particles. The interaction of silica particles with these polished surfaces will determine the level of particle contamination after Cu CMP.

In this paper, the interaction forces, between particles and surfaces were calculated

based on DLVO theory at different pH ranges [3]. Also, experimental measurements of adhesion forces between them were performed using an AFM. The magnitude of particle contamination on Cu, TaN and TEOS surfaces was observed after polishing them in order to confirm the calculated and measured interaction forces.

EXPERIMENTAL MATERIALS AND PROCEDURES

For the experiment, TEOS (Tetraethylorthosilicate), TaN and Cu deposited wafers were used as substrates. TEOS wafers were cleaned in the mixture of H_2SO_4 and H_2O_2 (4:1) followed by DHF treatment. The semiconductor-grade wet chemicals were provided by Dong Fine Chem. Co. and used for the experiment. The zeta potentials of all materials used in this study were measured as a function of pH. Zeta potentials were analyzed using a LEZA 600 (Otsuka Electronics) zeta potential analyzer. The adhesion force has been measured by analyzing the force on the cantilever as a function of distance between cantilever and surfaces using an Atomic Force Microscope (AutoProbe® CP Research, Park Scientific Co.) in liquid. The adhesion force was measured in solution as a function of pHs in 10^{-3} M KCl solutions using an electrochemical liquid cell. For the interaction force measurements, a glass particle of a radius of 20 μm (Duke Scientific Co.) was attached on a tipless AFM cantilever. Figure 1 shows the optical micrograph of a silica particle on the tipless cantilever. The wafers were polished with silica particles on a polisher. (PM5 polisher, Logitech Co.) The rotation speeds of the head and platen were set at 30 rpm. The pressure of the carrier was 3 psi. Polishing time was set for 1 min. A constant slurry flow rate of 120 ml/min was used for the polishing. For the preparation of slurry, the shaker and ultrasonic power were applied for 60 min and 30 min, respectively. Copper CMP slurry was prepared by mixing 10 wt% fumed silica abrasive and corrosion inhibitor (BTA, 10^{-2}mol) in 10^{-3} KCl solutions, which is the same used for AFM measurements. The polished wafer surfaces were observed by FESEM for the particle contamination.

RESULTS AND DISCUSSIONS

The zeta potentials of slurry particles and wafers were measured as shown in Figure 2. The zeta potential of Cu surface was analyzed with that of Cu particle because the zeta potential of general metal surface could not be measured due to the high conductivity and cell constant.

DLVO theory estimates the repulsive and attractive force due to the overlap of electric double layers and London-van der Waals force in terms of inter particle distance, respectively. The fundamental interactions occurring between particles and the wafer surface in solution are the van der Waals force(V_A) and electrostatic force (V_R) as shown in equation [4].

$$V_T = V_A + V_R \qquad (1)$$

If a small interparticle separation is assumed, van der Waals forces for a sphere and substrate can be expressed to

$$V_A = -A_{123}\frac{R}{6H_0^2} \quad \text{where,} \quad (A_{132} = (A_{11}^{1/2} - A_{33}^{1/2})(A_{22}^{1/2} - A_{33}^{1/2})) \qquad (2)$$

A_{132} is the Hamaker constant of two particles 1 and 2 in dispersion medium 3 and calculated based on A_{11} value and R is the radius of a sphere. The Hamaker constants of unknown metals were calculated based on their definition as shown below

$$A_{11} = \pi^2 n^2 C_1 \cong 3/4 h\nu (0.1)^2 \qquad (3)$$

Where n is number of atoms per unit volume, C_1 is (3/4) $h\nu_0\alpha_2$, $h\nu_0$ is ionization potential and α is polarizability. Hamaker constants used for this study were summarized in Table1.

Table 1. Hamaker constants used for van der Waals force calculation

Materials	A_{11} ($\times 10^{-20}$ J)
Si	25.6 [5]
SiO_2	50 [5]
Cu	28.4 [6]
TaN	25.9 *

* = based on eq.(3)

The calculation of electrostatic force due to the overlapping of the diffuse double layer between two surfaces is complex. It must rely on numerical solutions or various approximations. Overbeek's approximation [7] was used for the calculation of electrostatic forces due to diffused double layer interaction as shown in below.

$$V_R(H) = \frac{64\pi\varepsilon a_1 a_2 k^2 T^2 \gamma_1 \gamma_2}{(a_1 + a_2)e^2 z^2}\exp[-\kappa H] \qquad \text{where,} \qquad \gamma = \frac{\exp[ze\psi_d / 2kT] - 1}{\exp[ze\psi_d / 2kT] + 1} \qquad (4)$$

where z is the counter ion charge number, a_1 and a_2 are particle radius, κ is $(8\pi n\nu^2 e^2/\varepsilon kT)^{1/2}$.

Figure 3 shows the DLVO total interaction energy between a silica particle and wafers as a function of pHs. The stronger attractive force was calculated for silica particles and wafers in acidic than in alkaline solution. In acidic, neutral and alkaline solution, attractive interaction force between silica particle and TaN wafer was the strongest, attractive interaction force between silica particle and SiO_2 wafer was the weakest.

The change of interaction force between the particle and surface was measured as

the cantilever approached to the substrate [8]. The AFM probes the surface of a sample with a sharp tip, a couple of microns long and often less than 100 Å in diameter. The tip is located at the free end of a cantilever that is 100 to 200 μm long. Forces between the tip and the sample surface cause the cantilever to bend or deflect. A detector measures the cantilever deflection as the tip is scanned over the sample. Several forces typically contribute to the deflection of an AFM cantilever. The force most commonly associated with atomic force microscopy is an inter-atomic force called the van der Waals force. Figure 4 shows a typical force-versus-distance curve or force curve. Force curves show the deflection of the free end of the AFM cantilever as the fixed end of the cantilever is brought vertically towards and then away from the sample surface. Figure 4 (a) shows the cantilever shapes at several marked along the force curve. (A) in Figure 4 (b) is with the movements cantilever at each point. In the case shown, there is minimal long-range force, so this part of the force curve shows no deflection. (B) in Figure 4 (b) is that as the probe tip is brought very close to the surface, it may jump into contact if it feels sufficient attractive force from the sample. (C) in Figure 4 (b) is that once the tip is in contact with the surface, cantilever deflection will increase as the fixed end of the cantilever is brought closer to the sample. (D) in Figure 4 (b) is that after loading the cantilever to a desired force value, the process is reversed. A key measurement of the AFM force curve is the (C) in Figure 4 (b) at which the adhesion is broken and the cantilever comes free from the surface. This can be used to measure the rupture force required to break the bond or adhesion. The bigger the jump out point, the more attractive interaction force [9].

Figure 5 shows the measured interaction forces between particles and surfaces. Figure 5 (a) shows the interaction forces in alkaline solution of pH 11. The attractive forces of SiO_2, Cu and TaN wafers were measured to be – 0.776 nN, – 2.019 nN and – 2.04 nN, respectively. The strongest interaction force on TaN wafers and the weakest interaction force on SiO_2 were measured. Figure 5 (b) shows the interaction forces in neutral solutions. The attractive forces of SiO_2, Cu and TaN wafers were measured to be – 4.977 nN, – 14.456 nN and – 15.11 nN, respectively. The attractive force in acidic solutions was relatively stronger than alkaline solution on all wafers. Figure 5 (c) is the measured of the interaction forces in acidic solution. The attractive forces of SiO_2, Cu and TaN wafer were measured to be – 10.1 nN, – 18.78 nN and – 20.18 nN, respectively. The attractive force in acidic solutions was the strongest among solutions with different pHs. In all pHs the measured interaction force showed the same results as calculated one. TaN surfaces tend to have the strongest adhesion of silica particles in all pH ranges even though there are significant differences in their magnitudes.

In order to know how much the interaction force is important in the development of post CMP cleaning process, the wafers were polished with silica particles on a polisher. The least number of particles were found on the Cu wafer when polished alkaline slurry and the greatest on TaN wafer in using acidic slurry. It indicates that the interaction force plays a major role in determining the level of contamination on wafer surfaces during CMP.

SUMMARY AND CONCLUSIONS

The zeta potentials of slurry particles and wafer surfaces were measured to calculate

the total interaction force between them based on DLVO theory. The strongest attractive force was calculated between silica particle and TEOS, Cu and TaN wafers in acidic, neutral and alkaline pHs. Even the repulsive forces were calculated on TEOS, Cu, TaN wafers in alkaline pH. However, the strong attractive forces were calculated in other pH ranges. The adhesion force was measured between silica particle on cantilever and wafers by AFM. It was found the strongest adhesion of silica particles on TaN surface and the weakest on SiO_2 surface. As a result, both the calculated and the measured interaction forces were agreed well each other. In other to compare these results, particles on substrates were observed by FESEM after CMP. The least number of particles was observed a SiO_2 wafer and the greatest on TaN. The particles on Cu wafers were more difficult to remove than those on other wafers. Alkaline slurry was more desirable for a better control of particles on wafer surfaces after CMP than acidic slurry.

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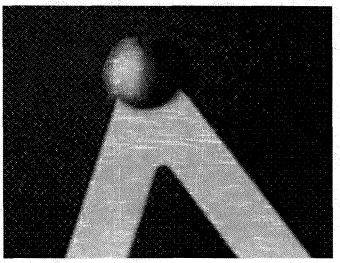

Figure 1. The optical micrograph of a silica particle on a tipless cantilever

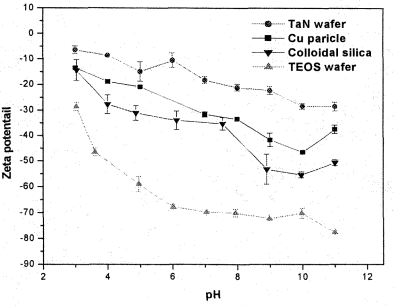

Figure 2. The zeta potential of Cu and colloidal silica particles and TEOS and TaN wafers as a function of solution pH

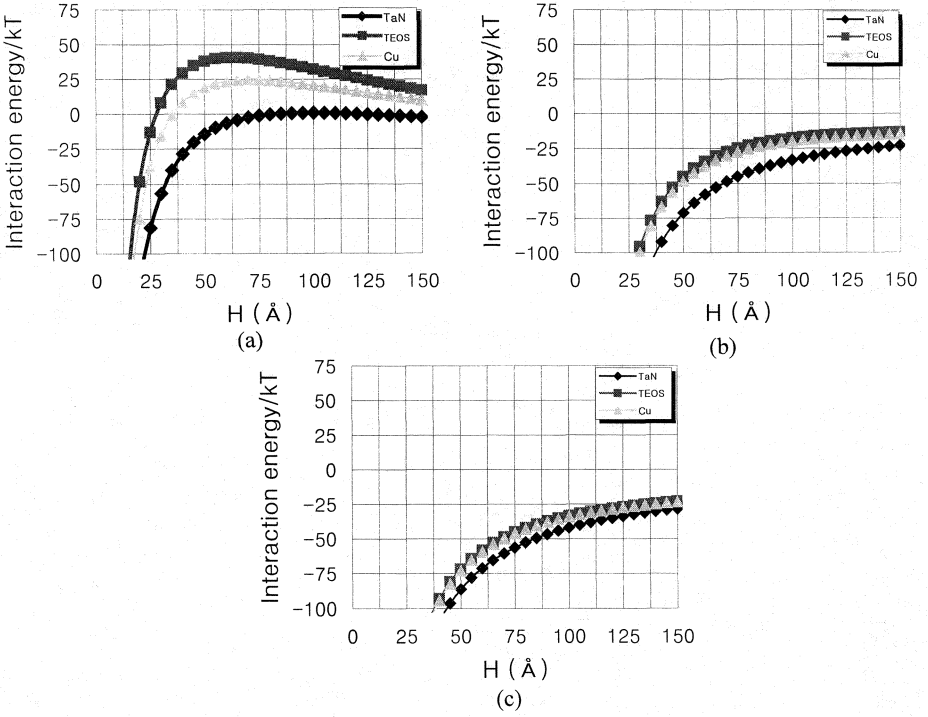

Figure 3. DLVO total interaction energy between silica particle and wafers at (a) pH 11, (B) pH 7 and (c) pH 3

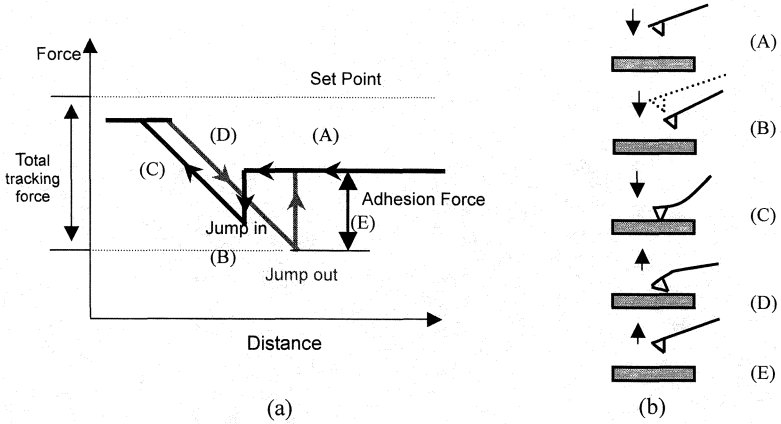

Figure 4. The change of (A) force curve and (B) cantilever shape as a function of applied force on a cantilever

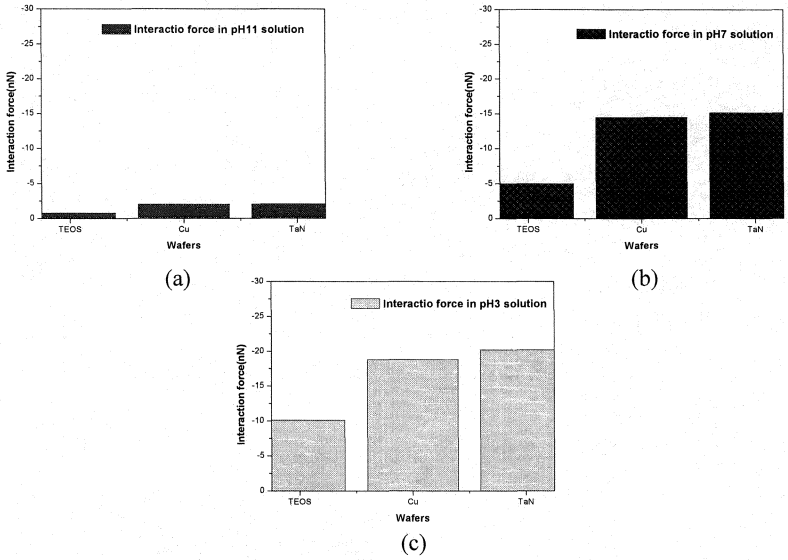

Figure 5. Interaction forces between silica particles and TEOS, Cu and TaN wafers measured in solution of (a) pH 11, (b) pH 7 and (c) pH 3 by AFM

OPTIMIZATION OF A BRUSH SCRUBBER FOR NANO-SIZED PARTICLES

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The article describes the optimization of a brush scrubber clean for nano-sized slurry particles. The removal of Clariant SiO_2 slurry particles with average size of 35nm from nitride substrates was studied, and the removal efficiency was determined. To measure nano-sized particles on wafers, the haze signal was used instead of the individual light point defects. The cleaning was done using a single double-sided brush cleaning station followed by a Lineagoni ^{TM} dry on a Damasclean ^{TM} tool from Mattson. The effect of different process parameters, which were varied using a design-of-experiment software, upon the particle removal efficiency is evaluated. The brush-wafer distance appears to be the most important parameter, and is further optimized. Finally, the brush loading effect was investigated with substrates highly contaminated with slurry particles. This effect can be greatly decreased by using adequate chemistries such as diluted NH_4OH.

INTRODUCTION

With shrinking dimensions of the IC structures, the impact of particles upon device yield becomes more and more important. To ensure high device yields, wafer surface contamination and defects must be monitored and controlled at several points in the semiconductor manufacturing process. Brush scrubbers are among the tools used to achieve such control and they have become one of the dominant instruments for wafer cleaning applications nowadays. Although we can find some publications about the principles of brush scrubber clean (1), the detailed analysis and optimization of it are not well reported, especially for nano-sized particles. Counting the nano-sized particles depositing on substrates is a big challenge because the state-of-the-art instruments allow only inspection of particles down to 80nm (KLA-Tencor SP1 ^{TBI}) or 50nm (SP1 ^{DLS}). However, it has been reported that the haze signal can be used in order to monitor high-density particles on a wafer surface (2, 3). This article describes the evaluation and optimization of a brush scrubber for the removal of nano-sized particles. The particle removal is determined on nitride and thermal oxide substrates using different particles.

The brush loading with particles during brush scrubber clean is investigated by processing highly contaminated wafers.

EXPERIMENTAL

An overview of the different particles used is given in Table I. Particle removal is studied on 200mm nitride wafers with 150nm nitride layer on 15nm pad-oxide and 200mm thermal oxide wafers with 500nm thermal oxide layer.

Table I: Overview of particles used and purchasing details.

Particle	Size (nm)	Vendor
Clariant Klebosol PL30S25 (SiO_2-slurry)	35 ± 10	Clariant
Si_3N_4	100 ~ 200	Alfa Johnson
Rodel ILD1300 (SiO_2-slurry)	100 ~ 200	Rodel
Cabot EPC4200A (Al_2O_3-slurry)	100 ~ 200	Cabot
PVPS - poly(1-vinylpyrrolidone-co-styrene)	~ 500	Aldrich
PSL - Polystyrene latex spheres	258 ± 20	Duke Sci.

After Imec-clean (4), wafers were intentionally contaminated with particles using an immersion based contamination procedure (approximately 4×10^4 Light Point Defects (LPDs)/wafer, measured in the range 0.1-0.2 μm). Particle contamination on the wafer surface is determined by light scattering measurements using a KLA Tencor SP1 [TBI] apparatus with a Dark Field Oblique illumination and a Wide collection configuration (DFWO). Particle Removal Efficiency (PRE) is calculated from the LPD counts or average haze signal before and after contamination and after the clean under investigation using

$$\mathrm{PRE} = \left(1 - \frac{\mathrm{After\_Clean} - \mathrm{Before\_Cont}}{\mathrm{Before\_Clean} - \mathrm{Before\_Cont}}\right) \times 100 \qquad [1]$$

Contaminated wafers were processed using PVA brushes (Texwipe TX5322) followed by a Lineagoni [TM] dry on Damasclean [TM] tool from Mattson. Prior to processing the particle-contaminated wafers, the brushes were preconditioned to have a negligible background of particles deposited on clean wafers using 2% dNH_4OH (pH ~ 12). The effect of different process parameters of brush scrubber such as brush speed, wafer speed,

brush-wafer distance, *pH* and cleaning time upon PRE was evaluated using a design-of-experiment software Echip6 with a linear design:

$$\text{PRE} = \text{Const.} + a_1 \times \text{Wafer\_speed} + a_2 \times \text{Brush\_speed} + a_3 \times \text{Brush-wafer\_distance} + a_4 \times \text{Cleaning\_time} + a_5 \times \text{pH} \quad [2]$$

with a_1, a_2, a_3, a_4 and a_5 the coefficients corresponding to the five process parameters. The settings used to vary the different process parameters are summarized in Table II.

Table II: Overview of process parameter ranges of design-of-experiment

Process parameter	Setting
Wafer speed	60 – 100 rpm(*)
Brush speed	150 – 300 rpm(*)
Brush-wafer distance	- 2.4 – -1.6 mm
Cleaning-time	10 – 91 sec.
pH	6 – 12

(*) Real values for wafer speed and brush speed corresponding to the set values when there is no brush/wafer contact. The Real values are much lower when the contact exists.

In order to optimize the brush-wafer distance, PRE is determined at different brush-wafer distances between –1.8mm and –2.6mm. When the brush-wafer distance is 0, the brushes just touch the wafer; the negative brush-wafer distances in this report mean that the brushes have contacted the wafer and are compressed on the wafer surface. In order to make a good comparison between different brush-wafer distances, the cleaning time was adjusted to have a fixed number of wafer rotations during the cleaning, *i.e.* 60 wafer rotations for each brush-wafer distance. As a control, after each particle-contaminated wafer, the particle counts are determined on a blank wafer to check for possible cross-contamination, which shows that there is no significant brush loading effect when low controlled contaminated ($\pm 4_{\times}10^4$ LPD/wafer) wafers are processed.

The effect of loading the brushes with particles was assessed by running nitride wafers highly contaminated with Clariant SiO_2 slurry particles (approximately $4_{\times}10^6$ LPD measured in the range 0.1-0.2μm). Totally one box of 25 wafers is processed, including 3 dummy wafers to precondition the brushes followed by a blank wafer to measure initial cleanliness of the brushes and 7 times a set of wafers consisting of 2 highly contaminated wafers followed by a blank.

The re-deposition of particles from brushes to wafers was investigated by contaminating the brushes with 5ml Clariant SiO_2 slurry particles. During the processing,

always the same recipe was selected: brush-wafer distance was set at -2.4mm and each wafer was cleaned with a fixed number of wafer rotations for each wafer processed (*i.e.* 60 wafer rotations/clean).

RESULTS

The removal efficiencies of different particles from thermal oxide and nitride substrates are summarized in Figure 1. In general, for most particles the removal efficiency is very high: the particle counts after brush cleaning are comparable to the levels obtained on 'clean' non-contaminated reference wafers. Whenever this is the case, the PRE is indicated as ~100 %. The SiO_2-slurry particles are found to be the most difficult challenge to remove. One further particle removal experiment was done using a patterned STI wafer contaminated with SiO_2-Clariant slurry particles after the CMP process. The wafer received a post-CMP brush scrubber clean using dNH_4OH. The particles were removed from thermal oxide field, but not from the nitride field (Figure 2).

Since the KLA-Tencor SP1 can not measure a real 30nm slurry particle but only measures in the tail of the particle distribution or particle agglomerates, an indirect method to measure the particles was used. The added average haze of the wafers as a function of the count of added LPDs between 0.1 - 0.2 μm on the wafers is depicted in Figure 3. The slopes of the linear fit are close to 1, showing that the haze of the wafer is proportional to the number of LPDs on the wafer. Using these curves, we can easily measure the number of particles depositing on the substrate indirectly by measuring the haze value of the substrate.

The effect of brush speed, wafer speed, brush-wafer distance, pH and cleaning time upon the removal of SiO_2 slurry particles from nitride substrates is summarized in Figure 4. The particle removal efficiencies are calculated using average haze values and LPD-counts in the ranges of 0.125-0.2 and 0.2-2.0 μm. In general, the particle removal efficiencies calculated using average haze values are smaller than the those calculated using LPD-counts for the small and the big range, suggesting that the small particles are relatively more difficult to remove compared to the bigger particles. Obviously, the brush-wafer distance is the most important parameter and is becoming more and more important as the particle size becomes smaller. Cleaning time is also important compared to the other process parameters. It also becomes more important as the particle becomes smaller. All the effects of other process parameters are minor compared to brush-wafer distance and cleaning time.

Since the brush-wafer distance is the most important parameter that influences the particle removal, it is further optimized. The particle removal efficiency calculated using

the haze of the wafer and the number of LPDs after brush scrubber clean as a function of brush-wafer distance are summarized in Figure 5. In general, particle removal efficiency increases when the brush-wafer distance becomes smaller. When it is reduced below -2.2mm, no real improvement is observed. For removal efficiencies determined using average haze values, they are close to 100%. However, when LPD counts between 0.1-0.2μm are used to calculate the removal efficiency, it is impossible to obtain 100% removal because of a rather high background addition of particles while the added haze on blank wafers amounts to zero. It is observed that an optimal removal is obtained if the brush is close enough (below -2.2 mm) to the wafer surface. The wafer rotation speed decreases greatly when decreasing the brush-wafer distance (see Figure 6) because of bigger friction between brushes and wafers. It can be easily concluded that the brush scrubber clean is a physical friction process.

Brush loading effects are assessed by continuously processing highly contaminated wafers, and the results are depicted in Figure 7. When UPW is used while processing the highly contaminated wafers, the particle removal efficiencies calculated using average haze values and LPD-counts decrease corresponding to an observed increase in added LPDs on the blank wafers (Figure 6a). These data show that the brushes can be contaminated when processing wafers with high particle contamination levels and the particles are released and re-deposit during further cleaning. This is also illustrated by processing a box of clean nitride wafers using the brushes intentionally contaminated with 5ml SiO_2 slurry particles. The first wafers processed have very high numbers of particles, which strongly confirm the re-deposition of particles from the brushes to wafer.

After processing the same wafers using dNH_4OH instead of UPW, the results are somewhat different (Figure 6b). The added LPD-counts on blank wafers processed with dNH_4OH in between the highly contaminated wafers are much lower than on blank wafers processed with UPW. The particle removal efficiencies for dNH_4OH are much higher than for UPW, especially when the average haze is concerned, in which case a removal near 100% is observed. It can be easily concluded that brush loading effects can be eliminated greatly by using the proper chemicals, such as dNH_4OH.

CONCLUSIONS

It is demonstrated that for high-density of nano-sized particles on a wafer surface, a linear relationship exists between the haze of the wafer and the added LPD-counts on the wafer. This haze signal can be used to study these very small particles that can not be measured otherwise.

The effects of different process parameters that influence the particle removal efficiencies during brush scrubber clean are studied using design-of-experiment. The brush-wafer distance appears to be the most important parameter among the process parameters studied, which confirms that the brush scrubber clean is a physical mechanical friction process.

When wafers with high particle levels are processed, the brushes can be loaded with particles, which reduces the cleaning efficiency: when the brushes are contaminated, the overall removal efficiency decreases because of re-deposition of particles from brushes to wafers. However, if the proper chemicals, such as dNH_4OH, are used during the brush clean, these loading problems can be eliminated greatly.

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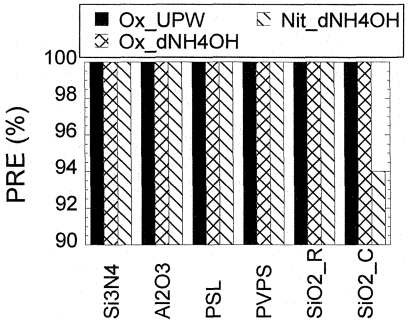

Figure 1: The particle removal efficiency (PRE) of different particles from nitride and oxide substrates using a UPW or dNH_4OH brush scrubbing clean.

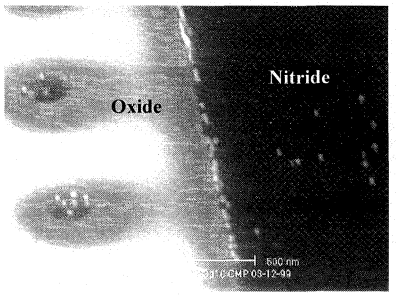

Figure 2: SEM picture of a patterned STI wafer cleaning by brush scrubbing using dNH_4OH after CMP.

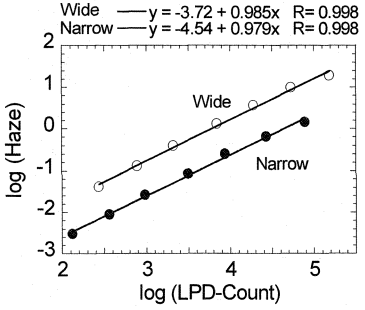

Figure 3: The haze measured on particle contaminated nitride wafers as a function of LPD-count on nitride wafers for both narrow and wide illumination (KLA Tencor SP1 measurements).

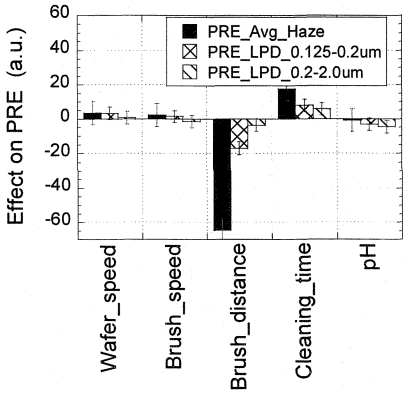

Figure 4: The effects of different process parameters upon particle removal efficiency during brush scrubber clean.

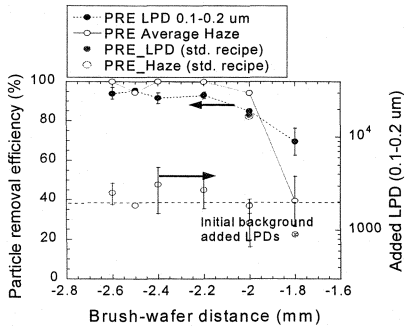

Figure 5: The particle removal efficiency calculated using haze and LPD-count *(left y-axis)* and the added LPDs on blank wafers *(right y-axis)* after brush clean as a function of brush-wafer distance.

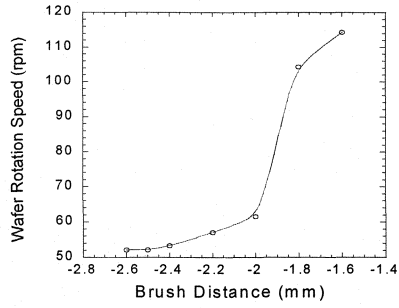

Figure 6: The wafer rotation speed as a function of brush-wafer distance.

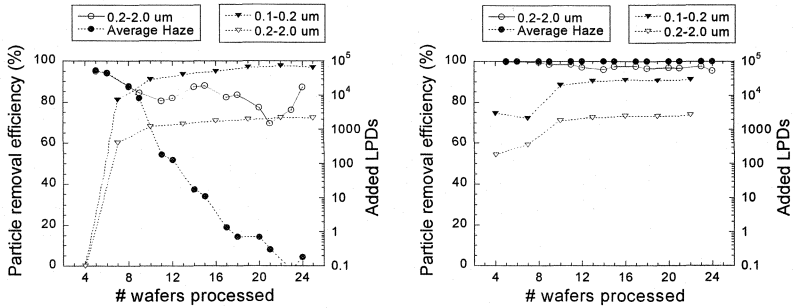

Figure 7: The particle removal efficiency *(left y-axis)* and the added LPD-counts on blank wafers *(right y-axis)* after processing wafers using brush scrubber clean with UPW (a) and dNH_4OH (b) on the scrubbers.

NATIVE OXIDE

INFLUENCE OF AMBIENT OXYGEN AND MOISTURE ON THE GROWTH OF NATIVE OXIDE ON SILICON SURFACES IN MINI-ENVIRONMENTS

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The influence of ambient gas concentration as well as wafer-storage time on the growth of the native oxide on silicon surfaces in a mini-environment has been investigated. The contribution of oxygen and moisture to the native oxide growth in the mini-environment is discussed based on equations to determine the rate constants in kinetics of the native oxide growth. The growth of the native oxide on silicon surfaces has been successfully suppressed by employing the hermetically sealed pod which can maintain the ambient oxygen and moisture in low concentrations without continuously purging the pod with nitrogen during wafer storage.

INTRODUCTION

As semiconductor devices continue to be highly integrated and their geometries also continue to shrink, not only trace organic contamination[1,2] but also thin native oxides on silicon surfaces have been shown to degrade device characteristics[3-5].

Native oxide grown on silicon surfaces has been shown to be able to cause incubation before film growth during low-pressure chemical vapor deposition[4] and to hinder the silicidation reaction[5] as well as epitaxial growth.

A silicided shallow junction in the low resistance source/drain of MOS transistors has been required to produce high-speed and low power transistors. Hence, a silicon surface in the source/drain is heavily implanted with dopants such as arsenic before the formation of a metal silicide. It is known that a native oxide grows extremely faster on the heavily doped surface than on a normal silicon surface[6-8]. Therefore, the growth of a native oxide on such surfaces should be stringently controlled.

Meanwhile, the native oxide grows on the surface of silicon wafers during wafer transport from the wafer-cleaning equipment to the film deposition equipment. Hence, silicon wafers must be isolated from cleanroom air which causes the growth of native oxides during wafer transport. The cleanroom air containing oxygen and moisture still exists in wafer containers even if silicon wafers are stored in wafer boxes or the standard mechanical interface (SMIF) pods.

It is known that the growth of a native oxide on a normal silicon surface is prevented by wafer-storage in nitrogen with no more than a 0.1 ppm moisture concentration[9]. However, it will not be feasible to maintain such a low concentration in mini-

environments, wafer stockers, or wafer containers for a prolonged period, and the effect of the wafer-storage in nitrogen on the native oxide growth on the heavily doped surface has not been reported.

In this study, we have investigated the relationship between the thickness of the native oxide and ambient gases, such as oxygen and moisture, as well as the elapsed time during wafer-storage in mini-environments to examine the inhibition of the native oxide growth from a practical point of view.

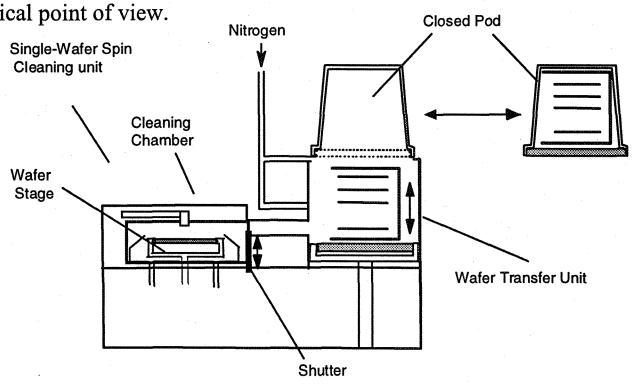

Figure 1. Schematic diagram of the nitrogen purged mini-environment system integrated with a cleaning unit.

EXPERIMENTAL

The mini-environment system we developed consists of a wafer-transfer unit and a hermetically sealed pod which can store 25 slices of 200mm-diam. wafers and is integrated with single-wafer spin-cleaning equipment, as shown in Fig. 1. It is capable of purging the interior of the system with nitrogen during transferring the silicon wafers to the pod. After wafer cleaning, the shutter between the cleaning chamber and the wafer-transfer unit is opened to transfer a wafer from the cleaning chamber to the transfer unit. The transfer unit is capable of keeping both oxygen and moisture concentrations in the wafer-transfer unit at no more than 0.1% by purging it with nitrogen.

The hermetically sealed pod used in most of the experiments consists of an aluminum body which has a flange and an aluminum bottom lid which has O-rings at its periphery to hermetically seal the pod when closed by keeping a vacuum in the gap between the flange and the lid[5]. The pod can be purged with pure nitrogen in order to replace the interior atmosphere with nitrogen and the concentrations of both oxygen and moisture in the pod can be less than 10 ppm within 10 minutes and 30 minutes, respectively, depending on the nitrogen supply rate.

An ordinary SMIF pod was also used for comparison with the hermetically sealed pod in terms of maintaining the ambient nitrogen and inhibiting the native oxide growth.

Silicon wafers used in this study were prepared from an n-type, 8-12Ωcm Czochralski crystal with (100) orientation. The silicon wafers were implanted with 40 keV arsenic ions to a dose of 3 x $10^{15}/cm^2$, and then subjected to rapid thermal annealing (RTA) in nitrogen at 1000 °C for 10 seconds to activate the implanted dopant impurities. Native oxides on the silicon surfaces were completely removed using a 3.6% HF solution in a cleaning unit equipped with the mini-environment system. The silicon wafers were then transferred to either a hermetically sealed pod or a conventional SMIF pod[10] in nitrogen through the transfer unit of the mini-environment without exposure to air immediately after the HF treatment.

The closed pod we newly developed or an ordinary SMIF pod was next purged with pure nitrogen until both the oxygen and moisture concentrations of the pod decreased to less than 10 ppm. After the pods were sealed and removed from the wafer-transfer unit, some groups of wafers were stored in the closed pod or the SMIF pod without additional nitrogen supply for one week after the pods were purged with nitrogen. The oxygen and moisture concentrations in pods during wafer storage were measured by a zirconia type oxygen analyzer and a capacitance type moisture analyzer, respectively. Another groups of wafers were stored in the closed pod where nitrogen containing different concentrations of oxygen and moisture was continuously supplied for one week. The flow velocity was 1 l/min. Other wafers were, as control samples, exposed to the atmosphere of the cleanroom without the mini-environment for several hours after the HF treatment.

The surface composition of the silicon wafers exposed to ambient air or stored in pods was analyzed by X-ray photoelectron spectrometry (XPS). The thickness of the native oxide on the silicon surface was computed from the intensity ratios of the Si 2p peak corresponding to the Si-O bonding and the elemental Si 2p attributed to the substrate using the take-off angle and the escape depth of the Si 2p photoelectron by assuming it stoichiometric. The take-off angle of the photoelectrons was 55° relative to the wafer surface normal in order to enhance the surface sensitivity. The escape depth of the Si 2p photoelectron from SiO_2 of 2.836 nm was used to compute the thickness.

RESULTS AND DISCUSSION

Figure 2 shows the change in the concentrations of both oxygen and moisture in a conventional SMIF pod and in a closed pod (a hermetically sealed pod) without additional nitrogen supply after these pods were purged with nitrogen. The concentrations of oxygen and moisture in the pods increased with time. This increase is considered to be due to the emission of absorbed water from the inner wall of the pods and permeation of oxygen from the exterior to interior of the pods through a gap between the flange and of pod lid. Both the oxygen and moisture concentrations in a conventional SMIF pod quickly increased close to the concentrations of the ambient air. In contrast, the concentrations in the closed pod slowly increased and seemed to saturate below a concentration of 700 ppm for both the moisture and oxygen.

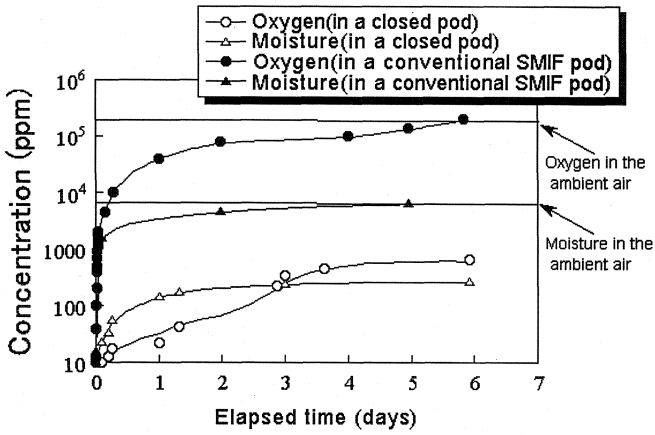

Figure 2. Time dependence of oxygen and moisture concentrations in two different types of pods.

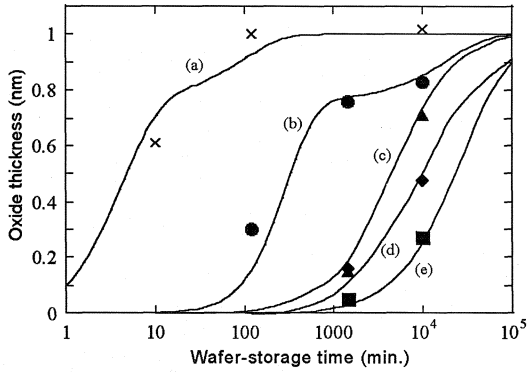

Figure 3. Time dependence of the thickness of native oxide grown in various environments: (a)in ambient air, (b)in 1000ppm oxygen and 1000ppm moisture in nitrogen, (c) in 1000ppm oxygen and 100ppm moisture, (d) in 100ppm oxygen and 1000ppm moisture, and (e) in 100ppm oxygen and 100ppm moisture.

Figure 3 shows the time dependence of the thickness of native oxides on the surface of silicon wafers stored in various environments. The native oxide growth is suppressed less than 0.3nm for two-hour or shorter storage times even if both the oxygen and moisture concentrations are maintained at 1000 ppm, in contrast, a native oxide grows to 1.0 nm to saturate within two hours in ambient air. The lower the concentrations of both oxygen and moisture in the pods, the slower the growth rate of the native oxide gets.

In other words, the growth rate of a native oxide depends on the concentrations of the oxygen and moisture as well as on the surface-exposure time. The rate constant of the growth of a native oxide is considered to be a function of the concentration of oxygen and moisture. Particularly, the oxygen concentration will significantly affect the oxide growth compared to the moisture concentration. This suggests that even plastic materials can be used as pod materials if adequate sealing methods to isolate the silicon surfaces from oxygen are developed, while plastics with a low water absorption rate should be chosen as the plastic pod materials. The influence of the concentrations of oxygen and moisture on the native oxide growth will be discussed based on the kinetics of the native oxide growth as follows:

The model suggesting that the oxidation in ambient air consists of two stages and is a first order process was proposed by T. Miura et al.[11]. Water molecules in the ambient air are adsorbed onto a silicon surface and covers the surface in the first stage.

At the first stage, the rate equation for moisture adsorption onto a silicon surface can be simply given by

$$d\theta_1/dt = k_1(1-\theta_1)\cdots\cdots(1)$$

where θ_1 is the coverage of the oxidized surface and k_1 is the rate constant.

Oxygen is consecutively adsorbed onto the surface on which moisture is adsorbed and diffuses into a silicon substrate to form Si-O bonds at the backbonds of the surface silicon atoms.

At the second stage, the rate equation for the oxide growth on a silicon surface due to the oxygen adsorption and diffusion can be given by

$$d\theta_2/dt = k_2(\theta_1-\theta_2)\cdots\cdots(2)$$

where θ_2 is the coverage of the laterally grown oxide layer and k_2 is the rate constant of the oxidation. The oxidation proceeds laterally on the surface until the thickness of the native oxide saturates during these stages. This saturation is explained by the incubation for oxygen penetration from the oxide surface into the silicon substrates[6].

According to T. Miura et al.[11], the first saturated thickness of a native oxide can be determined by the product of the first saturation value of the thickness and the oxide coverage(θ_2) obtained by integrating Eqs. (1) and (2). The oxidation curves exhibit plateaus about 0.76 nm where the oxide thickness saturates in Fig. 3. We assume that the first saturation value of the native oxides is about 0.76 nm based on a structural model of the silicon dioxide / silicon interface proposed by Herman et al.[12].

In addition, we considered the oxidation after the first saturation of the native oxide to determine the finally saturated thickness of the native oxide.

After the thickness of the native oxide first saturates, the rate equation for the further oxide growth on silicon surface due to the oxygen diffusion can be given by

$$d\theta_3/dt = k_3(1-\theta_3)\cdots\cdots(3)$$

where θ_3 is the coverage of the oxidized surface and k_3 is the rate constant. We assume that the final saturation value of native oxides is about 1.0 nm. We assume that the rate constant for the further oxidation after the initial saturation is about 1/200 that of first oxidation because the oxide growth rate is proportional to the inverse of the thickness of the already grown oxide [13].

Thus, the thickness of the native oxide on the arsenic heavily implanted silicon surface can be given by

$$T_{OX} = \theta_2(t) \cdot T_1 + \theta_3(t) \cdot (T_S - T_1) \quad \cdots\cdots(4)$$

where T_1 is the first saturated thickness of the native oxide and T_S is the final saturated thickness of the native oxide.

It has been reported that the growth rate of native oxides on silicon surfaces strongly depends on the humidity in the air in which silicon wafers are stored[11]. Our findings show that the oxygen concentration as well as the humidity have a significant influence on the growth rate and the decrease in the oxygen concentration is more effective for suppressing the oxide growth than the humidity. We considered the greater contribution of oxygen to the oxide growth to propose a model that the rate constant of moisture adsorption is a function of both the oxygen and moisture concentrations and the rate constant of the oxide growth due to oxygen diffusion after water adsorption is a function of only the oxygen concentration.

$$k_1 = 15 \cdot C_{H2O}^{0.6} \cdot C_{O2}^{0.8} \cdots\cdots(4)$$

$$k_2 = 0.01 \cdot C_{O2}^{2} + 10 \cdot C_{O2} + 0.001 \cdots\cdots(5)$$

$$k_3 = 5 \cdot 10^{-3} \cdot k_2 \cdots\cdots(6)$$

where C_{H2O} and C_{O2} are the moisture and oxygen concentrations in ambient nitrogen, respectively. Equation 4 shows that oxygen can contribute to the moisture adsorption onto silicon surfaces. It is considered that the oxidation on the top surface due to oxygen adsorption plays a role in accelerating the moisture adsorption onto the silicon substrates. The thickness of the oxide grown on silicon surfaces under ambient conditions with five different kinds of constant concentrations of oxygen and moisture based on Eqs. (1), (2), (3), (4), (5), and (6) are calculated with the initial conditions of $\theta_1=\theta_2=\theta_3=0$. The values of the calculated oxide thicknesses are plotted as a function of elapsed time in Fig. 3. This model is almost consistent with the experimental results.

For the general use of nitrogen-filled pods, both the oxygen and moisture concentrations in the pods are not constant, but they change with time, as shown in Fig. 2. This shows that the rate constants themselves depend on the elapsed time based on the change in both the oxygen and moisture concentrations. The thickness of the oxide grown

on silicon wafers stored in a conventional SMIF pod or the closed pod filled with nitrogen are calculated based on Eqs. (1)-(6) and other equations obtained by the time dependence of both the oxygen and moisture concentrations in the pods shown in Fig. 2. The calculated values of the oxide thickness are plotted in Fig. 4. It shows that the simulated curves of thickness of the oxide grown in both pods have a sharp rise at certain storage times and the growth of the native oxide in the closed pod is retarded. The simulated curve satisfies the experimental value of thickness of the native oxide grown in a closed pod for one week.

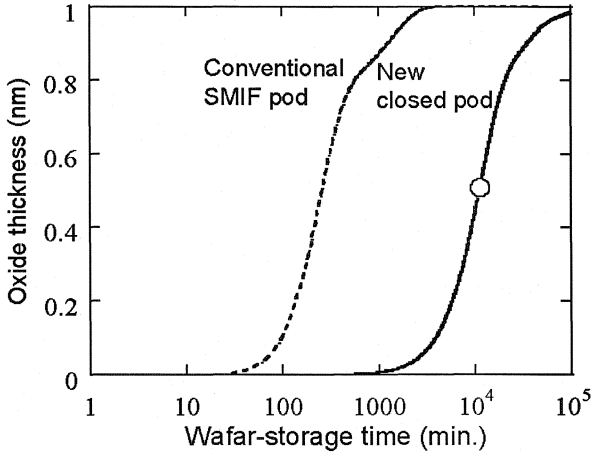

Figure 4. Relationship between the calculated thickness of native oxide grown on silicon substrates and the storage time in a conventional SMIF pod as well as the new closed pod.

SUMMARY

The influence of the oxygen and moisture concentrations as well as wafer-storage time in mini-environment pods purged with nitrogen, on the growth of the native oxide has been investigated. It has been found that the rate constant of the growth of the native oxide is a function of the concentration of both the oxygen and moisture.

Particularly, the oxygen concentration will be predominant in the growth of the oxide compared with the moisture concentration. Even plastic materials can be used as pod materials in mini-environments if adequate sealing methods to isolate the silicon surfaces from oxygen are developed.

The growth of the native oxide as well as the adsorption of organic contaminants on the silicon surfaces after wafer cleaning has been successfully inhibited by storing the silicon wafers in a hermetic pod purged with nitrogen.

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SPECTROSCOPIC AND ELECTROCHEMICAL STUDIES OF THE GROWTH OF CHEMICAL OXIDE IN SC-1 AND SC-2

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By combining spectroscopic and electrochemical measurements, the growth of chemical silicon oxide in oxidizing solutions SC-1 and SC-2 has been studied during several hours. On one hand, the SC-1 oxidation is always in quasi-stationary equilibrium between oxidation of the substrate and the dissolution of oxide layer. The analysis of the whole results shows that the structure of the oxide built is evolving. In the other hand, it was found that the growth in SC-2 is in agreement with a mechanism of a spreading oxide layer.

INTRODUCTION

In alkaline oxidizing solutions SC-1, the growth of a passivating oxide layer and its dissolution by hydroxide ions occur in the same time[1,2]. The mechanism of particle removal from the surface is based on this under etching. SC-2 solutions also oxidize the Si surface but the main difference is that the oxide formed is not soluble in acid media except for HF. The understanding of the chemical surface structure is taking most attention for different applications (High K, gate stack...) as it constitutes a more important part of the final material. In order to have a better comprehension of the structure and the growth of the chemical oxide, we have followed in situ by impedance spectroscopy (IS) and ex situ by optical techniques the surface evolution in SC-1 and SC-2 solutions. Chemical surface bonds were evidenced with ATR and ARXPS. The correlation between electrochemical, optical and spectroscopic methods for the characterization of the chemical oxide growth in these two medias are discussed in this paper.

EXPERIMENTAL

This study was carried out using p-type silicon wafers (boron doped, 10^{15} at/cm^3) (100) oriented, 200 mm diameter. The wafers were deoxidised by DHF 0.1% for 5min, rinsed in deionised water and oxidised in SC-1 or SC-2 solutions both at a ratio of 1:1:50 at room temperature or 65°C. An Opti-Probe Thermawave 5220 ellipsometer was used to monitor the thickness evolutions of the chemical oxide on bare wafers and the dissolution rate of thermal oxide (the refractive index of pure silicon

oxide n=1.46 has been assumed). The etch rate of the substrate was measured by spectroscopic ellipsometry using SOI substrates as described by Celler et al[3].

The electrochemical measurements were obtained by using an EG&G PAR Model 273A potentiostat and an impedance analyser Solartron 1260. The whole of our experiments were conducted in an electrochemical cell, described in a previous publication [4]. To follow the impedance variation versus time during the oxide growth, the frequency range was chosen to record one Nyquist plots in less than 2.5min, typically from 40 Hz to 0.05 Hz, which was checked to correspond to the oxide layer RC loop[5].

Angle resolved X-ray photoelectron spectroscopy (AR-XPS) and infrared spectroscopy in attenuated total reflection mode (ATR) were performed on the samples to extract structural information of the oxide layer. The XPS measurements were performed on SSI spectrometer equipped with a monochromatic Al Kα source at a take-off angle of 35° and a concentric hemispherical analyser. The ATR set up consists of a germanium prism pressed against the silicon sample. A p polarized IR beam coming from a Bruker IFS 55 FTIR spectrometer is directed on the prism base, with an angle of 71°, which ensures a total reflection on the germanium prism diopter.

RESULTS AND DISCUSSION

1) Oxide growth in SC-1 solutions

In SC-1, a limiting thickness is obtained immediately after the treatment and is increasing with the temperature from 6.6 Å to 7.5 Å (fig1). In the same time, the corrosion rate of silicon substrate was found to be 0.1Å/min at 25°C(fig2). The quasi-stationary state between oxidation and dissolution is immediately reached. The dissolution of thermal oxide is 0.03Å/min, strictly constant for more than 3 hours probing that the concentrations and temperature of the solution are constant during the experiment.

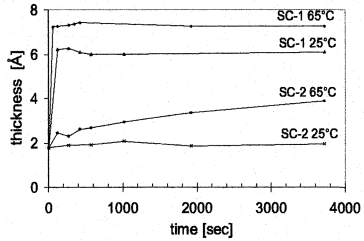

Figure 1: Optical thickness evolution during SC-1 and SC-2 oxidations

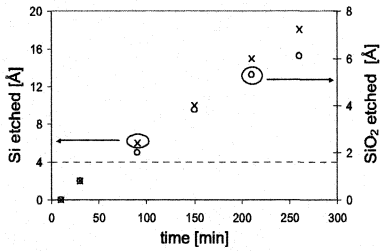

Figure 2: Dissolution rates of thermal oxide and Si substrate in SC-1 at 25°C

The Nyquist plots followed for more than 3 hours in SC-1 show that the shape of the semicircles increases with time (fig3) indicating that a silicon oxide is growing up on the surface. Experimental results fit an almost ideal RC circuit[5]. The polarization resistance R_P, which is equal to the charge transfer resistance R_T plus the ohmic drop through the oxide layer, is proportional to the diameter of the semicircles. It decreases rapidly during the first 30min and level off with time according to the diffusion of reactant through the oxide-protecting layer. After the first stage of 30min, Rp is slowly increasing (fig 2). The corrosion current is inversely proportional to R_T with the following relationship: $i_{corr} = RT / FR_T$ where R is the ideal gas constant, T the temperature and F the faraday's constant. The capacity of the oxide layer is decreasing and then reaching a plateau of 1 $\mu F/cm^2$. These results can be interpreted as resulting from higher insulating properties of the oxide with time.

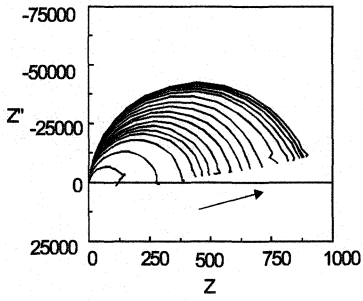

Figure 3: Nyquist plots for the oxide growth in SC-1 solution

The ATR spectra of figure 4 reveal that the surface oxidation by SC-1 treatment is evidenced by the 2 bands of the oxide network corresponding to the transverse (TO) and longitudinal (LO) mode of vibration of the Si-O-Si bonds[6] between 1000 and 1250 cm^{-1}. Moreover, the LO mode of the Si-O-Si bonds becomes more refined and is shifted of 20 cm^{-1}. This indicates that the oxide is more structured[7]. SC-1 oxidation also removes the surface hydrogen coating at early stages as shown by the disappearances of Si-H stretching vibrations between 2000 and 2300 cm^{-1}.

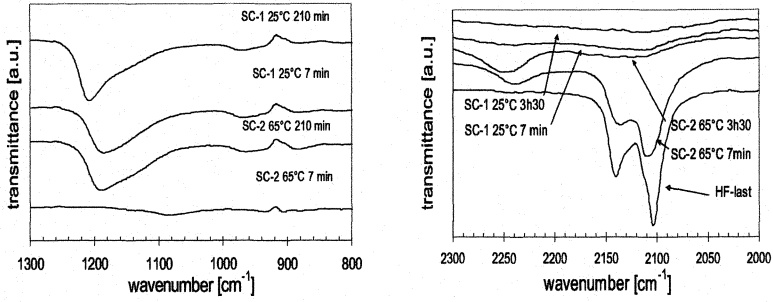

Figure 4: ATR spectra data in p polarisation for SC-1 and SC-2 oxides

The Si $2p_{3/2}$ spectra of the oxide surface show a main component due to the Si substrate and a broad one due to oxidized levels. These levels correspond to SiO_2 separated of nearly 4 eV with respect to Si-Si bonds and to other different suboxides SiO_x with a concentration of less than 10% of the total Si amount. With time, we have recorded an increase of the quantity of the SiO_2 bonds.

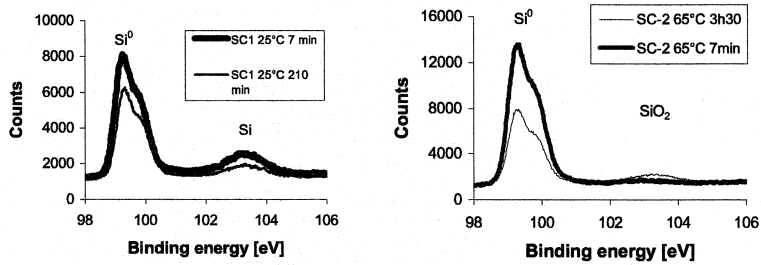

Figure 5: $Si2p_{3/2}$ spectra for SC-1 and SC-2 oxides at different time

The surface is continuously evolving because of the solubility of the generated oxide in alkali media, and both ATR and ARXPS data show that the oxide gets more structured. These results are in good agreement with the plateau of the capacity after 3 hours and also with the evolution of the Rp.

2) Oxide growth in SC-2 solutions

In SC-2 solution, the oxide is very slowly thickening at 25°C but grows following a logarithm shape at 65°C (fig 1). The Nyquist plots show that the center of the semicircles is not located on the real axis in SC-2 (fig 5). So the capacity of the oxide layer has been replaced by a non-ideal frequency-dependent capacitor called constant phase element (CPE). This behavior is generally attributed to heterogeneities of the current distribution at the surface. R_P is hundred times higher because of much higher insulating properties of the interface as compared with SC-1 at the same temperature.

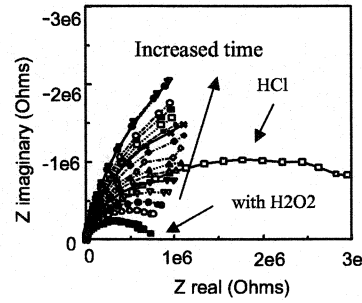

Figure 6: Nyquist plots for the oxide growth in SC-2 solution

In contrast with SC-1, the ATR spectra from figure 3 in SC-2 solutions at 65°C reveal that the oxidation takes longer time. For short treatment, low stretching vibration of the Si-O-Si bonds is visible while the Si-H bonds are not removed. After 210 min, the silicon back bonds are oxidized leaving O_3Si-H bonds on the surface and also Si-O-Si surface groups. XPS spectra (fig 5) show that the coverage is less than one monolayer for short SC-2 treatment [8]. This low coverage of the oxide layer and the presence of Si-H bonds evidenced by ATR show that the surface has a mixed structure. Thus, the CPE behaviour linked to heterogeneities of the current distribution at the surface could result from this mixed surface structure. The coverage is lower because the hydroxide peroxide H_2O_2 is less efficient in acidic media like SC-2 and also because the Si-Hx bonds are more stable. At longer time with SC-2 treatment, the results are in agreement with more coverage and suggest a mechanism of a spreading oxide layer. The growth of the chemical oxide can be thus modelled as island-like in SC-2 acid solutions.

CONCLUSION

IS has been applied to the evolution of the interface of silicon in SC-1 and SC-2 solutions. In SC-1, it allows a good comprehension of the interface evolution with the different electrochemical process involved. We have demonstrated that the silicon oxide gets more insulating with the variation of the electrochemical parameters and correlate to the change in the structure by spectroscopic and optical methods.

In SC-2, the mechanism of a spreading oxide has been evidenced both by the behaviour of the interfacial electrochemical properties and the characterization of the interfacial structural composition. The equivalent circuit is more complicated because the evolution of the Si-H bonds to an oxide layer takes longer time.

ACKNOWLEDGMENTS

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ELECTROCHEMICAL STUDY OF ULTRA-THIN SILICON OXIDES

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Wet ultra-thin silicon oxides, resulting from the oxidation of hydrophobic monocrystalline silicon surfaces in oxidizing cleaning solutions, were investigated with electrochemical methods. We used SC1 (NH_4OH: H_2O_2 : H_2O) and SC2 (HCl: H_2O_2 : H_2O) media, and the build-up of the silicon oxide on the surface was monitored in situ, by electrochemical impedance spectroscopy (EIS). In SC1 solution, the Nyquist plot reached a limiting semi-circle after *ca* 3 hours, leading to a resistance value tenfold less than in acidic SC2 solution, leading to the conclusion that the oxide layer was much more permeable to ions in SC1 electrolyte than in SC2 solution. Ellipsometric determination of the oxide thickness indicated that a limiting value was attained after only a few minutes in SC1 solution. These results let us to infer that the SC1 media affected both the thickness and the structure of the ultra-thin silicon oxide, a conclusion supported by infra-red spectroscopic investigations.

INTRODUCTION

Research in the field of ultra-thin silicon oxide layers commonly used in microelectronics industry as dielectric materials, was very active during these last years, because of the constant decrease of the elemental components dimensions. They are generally obtained by thermal oxidation at a temperature near 900°C. On the other hand, Si oxide is generated after a chemical treatment in an appropriate oxidizing solution such as SC1, ammonia solution, or SC2, acidic solution, currently used for many years to clean the silicon wafer surfaces, and get rid of inorganic and metallic nanoparticles (1, 2). These cleaning steps are carried before the thermal oxidation and the build up of a 12 Å thermal silicon oxide. Recently, it was demonstrated that the surface state resulting from the cleaning sequences could deeply influence the thermal oxide quality (3), and be responsible for dielectric breakdown. This is the reason why we aim at a better understanding of the growth mechanisms of the ultra-thin chemical silicon oxide resulting from the treatment in SC1 and SC2 solutions. We mainly used electrochemical investigation techniques, which were successful in our previous studies (4) to detect the

very first stages of silicon surface contamination. Mainly the open-circuit potential (OCP) and the electrochemical impedance spectroscopy (EIS), were used to follow in situ, the growth of the chemical silicon oxide on a bare hydrophobic surface, under zero current conditions. An equivalent circuit model leads to the electrical parameters of the layers, suggesting that the oxide grown in SC1 solutions is much more homogeneous than those grown in SC2. For a more accurate interpretation, these experiments were analyzed on the basis of other data such as ellipsometric and infra-red spectroscopic results.

EXPERIMENTAL

The monocrystalline silicon wafers were p- or n-type doped, (100) oriented, 200 mm diameter and mirror polished. The experiments were carried on in a specially designed electrochemical cell where the parameters leading to reliable results were carefully controlled. Most of the results were obtained in the dark at room temperature, and a few experiments were carried at 65°C to study the effect of an increase of the temperature.
The solutions were prepared using SLSI grade (Sub Large Scale Integrity, metal impurities below 1 ppb) reagents, NH_4OH (28%), HCl (37%), H_2O_2 (30%) diluted in ultra-pure water. The composition of SC1 mixture was (1 :1 :20) by volume and SC2 (1 :1 :50) either at room temperature or at 65°C.

The electrochemical parameters were reached by using an EG&G PAR potentiostat, model 273A, in connection with an impedance analyser Solartron 1260. Open-circuit measurements were recorded alternately with Nyquist plots, obtained in the frequency range from 100 kHz to 5.10^{-2} Hz, the amplitude of the sinusoidal signal being 10 mV, superimposed to the open circuit potential. An impedance spectrum was recorded, with such a configuration, in 2 min. 30 s. Then the SOE interface was modeled in terms of an equivalent circuit (fig.2) where resistance and capacity values were derived by fitting the experimental data to the model using the Zplot software included in the device.

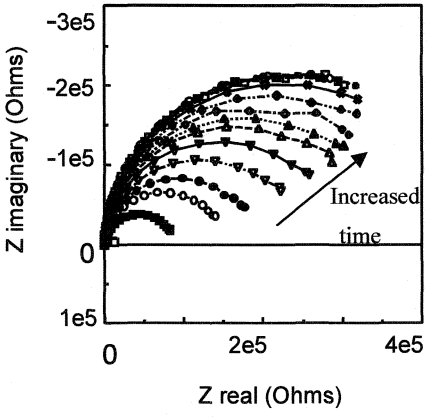

Fig.1 Sucessive impedance plots recorded on p-Si solution during 3h30min.

RESULTS

Oxide growth in SC1 solutions

We have investigated the behavior of a bare hydrophobic silicon surface in contact with the SC1 solution, during the chemical oxide growth. Impedance plots were recorded alternately with the simultaneous open-circuit potential variation. The duration of the experiments at room temperature was 3h30min to reach a steady state. The Nyquist diagram, representing the imaginary impedance component versus the real part, lead to well-shaped semicircles as indicated in the figure 1.
The experimental data from the diagrams were adjusted to fit at the best the equivalent circuit, as already proposed by Morrison (5), for the semiconductor/electrolyte interface. It is constituted of two (RC) parallel circuits, one related to the space charge layer of the semiconductor and the other to the SOE structure.

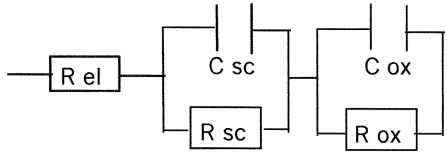

Fig.2. Equivalent circuit for the Si/electrolyte interface.

For p-type silicon samples, the contribution of the space charge layer was poorly visible, because the depletion process did not appear as the potential was shifted to more positive values. Only one semicircle corresponding to one RC time constant clearly appeared on the Nyquist plots. The charge transfert resistance, highly influenced by the oxide ohmic resistance, is equal to the diameter of the semi-circle, and was observed to gradually increase with time, as revealed by the successive diagrams on the figure 1 describing the evolution of the surface reactivity. The R and C components were assumed to directly depend on the thickness and the dielectric properties of the silicon oxide layer growing in the SC1 solution. Moreover, the center of the semi-circles was observed to be located on the real axis, indicating that the imaginary term identified as a constant phase element (CPE), could be considered as an almost pure capacitance. Indeed, this CPE is expressed as $Q\ (j\omega)^{-n}$ with $0< n < 1$. The coefficient n can be related to the uniformity of the dielectric layer controlling the electrochemical reactions on the surface. When the value of n is in the vicinity of 1, the equivalent component is identified as a pure capacitor. In our experiments concerning the Si oxide growth in SC1, n was found to be equal to almost 1 (0.98).

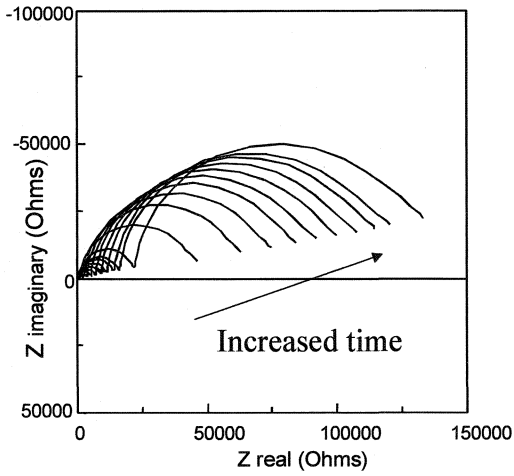

Fig.3 Nyquist plots recorded on n-type Si, in SC1 solution, in the dark

The impedance plots reported on the figure 1, reached a limiting diameter value after 3h30 immersion time in oxidizing ammonia solution (6, 7). The regeneration of the solution did not change significantly the impedance diagram, suggesting that a stationary regime was reached at this time, much more related to the surface oxide properties than to a possible change of the solution composition.

On the other hand samples of n-type Si were processed under quite the same experimental conditions. Then the evolution of the Nyquist plots showed a somewhat different behaviour due to the gradual emergence of a depletion layer with an icreasing impedance value as the potential gets more positive. The fig. 2 depicts the successive impedance diagrams, obtained in the dark, at zero curent potential. Two time constant appeared in this case. The first one, in the high frequency range, was attributed to the generation of a space charge layer within the silicon material due to the depletion of electrons near the interface. The second one was attributed to the passivating oxide layer, growing on the silicon surface during almost 3 hours. The R and C values associated to this second impedance loop were calculated and confirmed the similarity of the plots related to the oxide layer, in the case of p and n-type silicon. Such results suggested that both n- and p- type Si substrates have common properties connected to their chemical reactivity.

Oxide growth in SC2 solutions

A p-type Si sample was used to approach a better interpretation of the oxide growth mechanism, and of the effect of pH. A chemical oxide was built up in an acidic SC2 solution, (HCl, H_2O_2, H_2O), in the dark, at OCP. First the impedance plots of the bare hydrophobic surface were recorded in pure diluted HCl, and then, hydrogen peroxyde was introduced in the electrochemical cell. The Nyquist plots recorded as a function of time, are depicted in the figure 3. Upon the addition of H_2O_2 a sudden drop of the polarization resistance appeared showing the contribution of the electron transfer electrochemical reaction, and then was followed by a gradual increase of the impedance

related to the hindered access of reactants to the silicon surface through the generated silicon oxide.

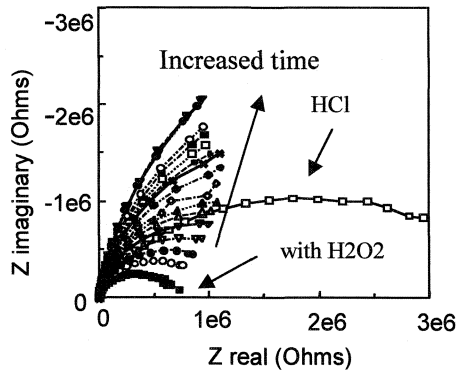

Figure 4 : Impedance diagrams evolution on p-type sample, in SC2 solution.

A steady regime was reached after more than 20 hours immersion time, indicating that the silicon oxide growth was much slower than in the case of SC1 media. Moreover, the constant phase element associated to each impedance loop was significantly different from 1 (typically 0.65) at the beginning of the oxide growth. This result suggested that the primary oxidation process lead to the formation of oxide nuclei. Thus the electrochemical properties could result from a mixed surface structure made of dielectric islands separated by an electrochemically active surface. It is interesting to note that as the Si surface coverage by the oxide increases, the n coefficient of the CPE approaches unity, and the SOE system behaves like an almost pure capacitor.

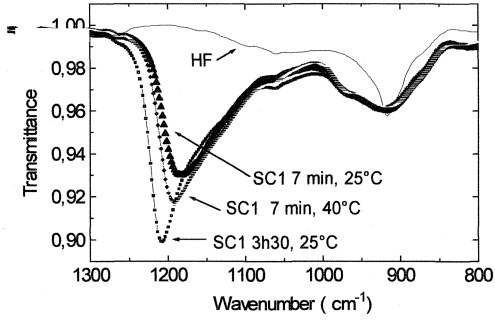

Fig.5 : Infra-red ATR spectra for Si oxides grown in SC1

All the results obtained in SC1 and in SC2, for both p- and n-type silicon substrates can be summarized as showing a gradual increase of the impedance during the chemical reaction with the oxidizing solution. Even though the mechanism is different in acidic solutions due to the insulating

properties of the oxide in acidic media, the general trend of the impedance growth could be assigned in a first approximation to a gradual increase of the oxide thickness. For this reason, the electrochemical experiments were complemented by independent determinations of the thickness value by ellipsometric measurements, for Si oxides grown both in SC1 and in SC2 as a function of the immersion time. Surprisingly, results obtained with a Opti-Probe Therma-Wave model 5220 ellipsometer were at variance with the facts observed by EIS studies although a qualitative agreement appeared in the comparison of SC1 and SC2 reagents. In fact during the treatment by the SC1 solution, ellipsometry indicated that the silicon oxide grown in SC1 at room temperature reached a limiting thickess value of 7.5 Å after just a few minutes. On the other hand the treatment by SC2 solution lead to approximately a 2 Å passivating layer thickness, reaching hardly 3 Å after 3 hours immersion time. Finally another test was necessary to decide whether the duration for the growing oxide to reach the steady state thickness is as long as derived by EIS diagrams or much shorter as indicated by ellipsometry. New informations came from the IR ATR spectra recorded with Si oxides grown in a SC1 solution at different time intervals. Fig.5 shows the main spectral peak at 1220 cm^{-1} assigned to the LO vibration of Si-O bonds in silicon oxide lattice. Fig. 5 clearly shows that this peak gets higher and sharper as time or temperature is raised, thus revealing a more ordered structure after 3h30mn treatment in SC1 at room temperature. Naturally, it is worth to recall that the EIS data were obtained *in situ* during the wet oxidation reaction, while ellipsometric measurements and infrared spectra were recorded under dry conditions after the samples were extracted from the SC1 solution.

DISCUSSION

It is generally accepted that the oxide growth in SC1 solutions results from two competing steps, one is the oxide generation by reaction with H_2O_2, the second being the simultaneous dissolution of this oxide in the ammonia alkaline solution. This mechanism takes place by dipping the wafers into the processing vessels, where the substrate is necessarily under zero current conditions. From our electrochemical experiments, the Si samples in SC1 are spontaneously submitted to the OCP whose value is shifted towards more positive values as a function of time. EIS measurements reval a simultaneous increase of the impedance values, *i.e.* a gradual lessening of the capacitance, together with a steep increase of the surface resistance. This resistance term must be assigned to a charge transfer at the interface. Indeed the zero current situation is generally considered as the resulting from exactly equal currents due to oxidation/reduction electron transfer reactions, so that the exchange current is directly related to the corrosion current through:

$$Rp = RT/(nF(\alpha + \beta)\, i_{corr})$$

where n is the number of electrons involved in the reaction, F the Faradaic constant, and R the perfect gas constant.

Several interesting informations can be derived from EIS measurements at the OCP. Indeed the reduction current of H_2O_2 being strictly compensated by the oxidation of Si

substrate, the corrosion current gives an evaluation of the loss of matter per time unit, the method leading to the silicon etching rate under the pre-existing oxide. We obtained an average value of 0.1 Å/min at room temperature in agreement with data obtained with a SOI structure by Celler et al. (7). Moreover this etching rate should decrease with time as the resistance component of the impedance gets higher, provided the conditions remain at zero current.

In a deeper analysis, we must recall that the higher value of R is tightly bound to the shift of potential to more positive values. In our electrochemical representation the OCP should be equal to the mixed potential resulting from two redox couples :

$$Si + 6\ OH^- \Rightarrow SiO_3^{2-} + 3\ H_2O + 4\ e^- \qquad E_1 \qquad (1)$$

$$H_2O_2 + 2\ e^- \Rightarrow 2\ OH^- \qquad E_2 \qquad (2)$$

As the Si oxide layer grows the variation of the resistance term can characterize the more or less hindered diffusion of the reactants to the Si substrate surface. The OCP is then given by the relation :

$$E_{(OCP)} = \tfrac{1}{2}(E_1 + E_2) + (RT/nF) \ln (i_{red}/i_{ox})$$

At this stage, the shift of the potential to more positive values should be interpreted as revealing a change of the Si oxide structure, resulting in more hindrance for the diffusion of Si-OH groups than for H_2O_2 molecules. Although *in situ* ellipsometric measurements are desirable, this remark can be a sound explanation of the apparent discrepancy between EIS and ellipsometric measurements. Our studies on the electrical properties of Si oxides (8), evidenced that the primary generated silanol Si-OH groups are partly ionized in alkaline solutions as $Si\text{-}O^-$ bringing the conductance properties of these systems. But with time, it is likely that most of the silanol groups will be transformed into siloxane Si-O-Si bridges, leading to a more ordered lattice structure, and making more difficult the diffusion of these oxidized species. Such an interpretation, supported by the IR spectra of fig. 5, makes a reliable synthesis of the whole experimental results.

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DRY CLEANING

A SURFACE CHEMISTRY APPROACH TO THE DEVELOPMENT OF GAS PHASE WAFER CLEANING PROCESSES

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Transmission FTIR was used to investigate the removal of residue layers on doped oxide films and to monitor the etching mechanism of thermal oxide films in real time. Partial removal of the residue on BPSG films containing a mixture of boric and phosphoric acids was possible with a low pressure/low temperature UV–Cl_2 process. Both direct and indirect UV illumination removed a portion of the residue, but the direct process produced an opaque residue on the surface of the doped oxide that could not be rinsed off immediately afterward. In low pressure HF/vapor etching of thermal oxide films, HF hydroxylates and fluorinates the Si surface atoms during the induction time forming groups of H-bonded silanols. After induction, etching begins when HF attacks $SiF_2(OH)_2$ moieties, which contain weaker Si–O bonds than in siloxane, producing molecular water which activates the oxide surface and SiF_4, which is volatile.

INTRODUCTION

The International Technology Roadmap for Semiconductors (ITRS) (1) identifies technical challenges for front-end of line (FEOL) surface cleaning in the areas of particle removal, hydrophobic and hydrophilic surface termination, and high κ compatible cleans. Options for both liquid and gas phase FEOL cleaning processes are shown in Table 1. Liquid phase cleaning is a mature and robust technology that offers the advantages of an aqueous solvent medium and high throughput, but is resource intensive. In addition to liquid chemicals, this process requires large amounts of water (60-80 million gallons per month for 20,000 wafer starts), cleanroom space for benches, and energy to run exhaust blowers. Moreover, wafer cleaning and CMP are the only semiconductor manufacturing processes that are carried out in a liquid phase, making them difficult to integrate with vacuum-based steps.

Gas phase or dry cleaning processes offer the potential to reduce the environmental impact of wafer cleaning in the fab and provide technology options for the next generation of front-end processing. Compared to aqueous based cleans, dry cleans improve narrow geometry penetration, use much less chemistry, are vacuum compatible, and, in principle, use little or no water (2). In spite of these obvious benefits, gas phase cleaning has not developed as initially envisioned due in large part to the continued improvement in liquid phase cleaning technology to meet industry needs. However, several developments are driving new cleaning strategies. These include larger wafer

sizes, single wafer processing in cluster tools, the introduction of new materials in device manufacture, environmental regulations set by government and environmental targets set by the ITRS Roadmap, and the increasing demands on contamination control and the associated rise in the number of wafer cleaning steps (3,4). The new cleaning strategies frequently incorporate dry cleans used in combination with aqueous based cleans for final surface conditioning before deposition. Whether dry cleaning is used to complement liquid phase cleaning or replace it, knowledge of the chemistry of gas/solid surface reactions is key to process and reactor design as well as process control and optimization.

Table 1: FEOL Surface Cleaning Challenges and Processing Options Adapted from 1999 ITRS (1).

Challenge	Processing Options	
	Liquid Phase	Gas Phase
Particle Removal	Dilute Chemistries Alternative Chemistries	Cryo Aerosol Laser
Hydrophobic Surface Termination	Integrated Final Rinse/Dry pH Adjusted Rinses Modified HF Chemistry	HF/vapor UV-Cl_2
Hydrophilic Surface Termination	SC-1 + Chelating Agents Ozonated DIW Rinses	Ozone UV-Ozone
New High κ Dielectrics	*Under development*	*Under development*

Two projects each of which involves etching silicon dioxide films demonstrate the potential benefits of understanding the surface chemistry. The first examines the removal of etching residues formed on doped oxide films. Doped SiO_2 films are used as insulating and sacrificial layers in the manufacture of microelectronic and MEMS devices. Gas phase HF etching of these films produces a residue with a low volatility. The residue layer is typically rinsed off with water before further processing. This water rinse, depending on the type of device structure produced, is often followed by an alcohol and/or supercritical CO_2 rinse and drying. The development of a completely gas phase etching process sequence for doped oxides would eliminate these extra rinsing steps, thus decreasing the waste produced and, potentially, the processing time. Previous work has shown that the primary etching products in the residue on borophosphosilicate glass (BPSG) films are a mixture of phosphoric, H_3PO_4, and boric, $B(OH)_3$, acids and water (5). A UV-Cl_2 process has been investigated using transmission Fourier transform infrared (FTIR) spectroscopy that removes a portion of the mixed acid residue. The second project examines the mechanism of etching thermally grown SiO_2 films using a mixture of anhydrous HF and water vapor with *in situ* FTIR spectroscopy done in real time. Previous studies have identified an induction time for oxide etching to begin, mass transfer and film charging effects, and various etching regimes using water and alcohol vapor (6-12). The results presented in this study suggest that HF attacks siloxane (Si–O–Si) bonds during induction producing groups of H–bonded silanols (SiO–H). After the induction period, etching of the SiO_2 lattice starts when HF attacks a Si atom that has bonds to F and OH, that is, no siloxane (Si–O–Si) bonds.

EXPERIMENTAL

Doped Silicon Dioxide Etching

Etching of as deposited BPSG (4.0 wt% B and 3.5 wt% P) films on 200 mm wafers in a commercial etching tool (Excalibur ISR, FSI International) has been described in detail elsewhere (5). The BPSG films used in this study were nominally 5000 Å thick and deposited by plasma enhanced chemical vapor deposition at 350°C on a 2000-2400 Å tetraethoxysilane (TEOS) buffer layer, then annealed at 500°C for 60 min. The films were etched at 55°C in a FSI Excalibur ISR tool at approximately 1 atm with a process consisting of a 120 second purge of 60 SLM of 55°C N_2, followed by a 400 s etch step by adding 0.05 SLM of anhydrous HF to the 60 SLM N_2 flow. This process etched approximately 3000 Å of the BPSG layer and produced a residue layer approximately 1000 Å thick. The wafers were removed immediately after etching from the Excalibur without rinsing, and diced manually into 1.5 cm x 1.5 cm samples. The samples were mounted on stainless steel pucks and processed in a research cluster apparatus by transfer at 10^{-8} Torr through a load lock to a vertical hot wall quartz tube reactor with a diameter of 35 mm. Samples were processed at 750 mTorr in the hot wall reactor at temperatures from 20 to 200°C in gas flows containing N_2 (from liquid boil off) and Cl_2 (99.998% VLSI-grade, Air Products) and illuminated with ultraviolet (UV) light produced by a high pressure Xe arc lamp (Spectral Energies, 1000 watts) located 20 cm from the outside of the quartz reactor. Either direct UV illumination perpendicular to the sample face or indirect illumination parallel to the sample was possible. Sample temperature was calibrated to the outside wall temperature of the quartz tube near the reaction zone in separate experiments. The UV lamp heated the sample differently in perpendicular and parallel orientations, which was accounted for in the calibration. Transmission FTIR spectroscopy scans of samples were taken before and after processing in the N_2-purged compartment of a Nicolet Magna 760 spectrometer at a 30° angle of incidence using a MCTA detector. All FTIR spectra were referenced to a clean, bare Si sample and baseline subtracted, and gas phase water peaks were subtracted.

HF/Water Vapor Etching of Thermal Silicon Dioxide Films

The etching of thermal silicon dioxide films was carried out in a reactor using a mixture of HF and water vapor and probed with *in situ* FTIR spectroscopy in real time. The samples were cleaved from a 200 mm double-sided polished wafer into 5 x 2 cm pieces. The pieces were dipped into a dilute HF solution and oxidized in a furnace at 1000°C using dry O_2 to grow a film 2000 Å thick. Following oxidation, the samples were cleaned with a standard liquid phase SC-1, SC-2, and Piranha sequence and rinsed with ultrapure water. A sample was mounted on a transfer puck and moved to the HF/vapor reactor through the research cluster apparatus under 10^{-8} Torr vacuum. The sample was aligned to allow the infrared beam from a Nicolet Magna 760 FTIR spectrometer to pass through one edge of the Si sample, reflect off of the stainless steel process gas showerhead, and pass through the other edge of the Si sample to a remote MCTA

detector mounted just outside of the reactor. The infrared beam was passed into and out of the reactor through ZnSe windows purged to keep process gas from condensing. This unconventional FTIR path probed the gas phase directly above the sample surface as well as both the Si sample and process gas showerhead surface. A gas handling system under computer control using LabView delivered metered amounts of process gas to the reactor. The LabView control system also allowed HF and water to be introduced into the gas flow without disturbing the pressure in the reactor ($\Delta p < 0.2$ Torr). FTIR spectra were recorded as a function of time during the flow of process gases into the reactor.

RESULTS AND DISCUSSION

Removal of Doped Silicon Dioxide Etching Residues

Anhydrous HF (AHF) etching of 500°C annealed BPSG films at 55°C produced a stable residue on the surface of the film approximately 1000 Å thick that contained a mixture of phosphoric acid, boric acid and water. The transmission FTIR spectrum shown in Figure 1a contains vibrational features at 2866, 3330, 3445, and 3650 cm^{-1} which are indicative of the PO–H (13), BO–H (5), HO–H (14), and SiO–H stretches of H–bonded silanols (15), respectively. The O–H stretches at 2334 and 3060 cm^{-1} have not yet been identified. The spectrum in Figure 1a was taken 10 min. after etching and changed shape over time from 6 hr to 3 days with storage in a wafer box in the cleanroom as shown by spectra b–d. A clean Si surface was used as a background for all spectra. The changes are marked by a loss of boric acid from the film and a shift in the 3330 cm^{-1} peak to lower frequency, which indicates a weakening of the bond, likely a result of increased hydrogen bonding due to uptake of water by the film.

A water rinse removes the acid residue leaving adsorbed water on the surface. The FTIR spectrum of a sample 2 hr after AHF etching and a sample 2 hr after etching and rinsed with ultrapure water for 20 s at 20°C in the cleanroom are shown in Figures 2c and 2e respectively. The rinse removes both the boric and phosphoric acids as shown by the absence of the BO-H and PO-H stretches. The SiO–H groups are unaffected by the rinse, and the broad peak at 3445 cm^{-1} is indicative of molecular water on the surface. The residue can also be removed by heating either in the cleanroom or under vacuum but a temperature of approximately 180°C over 1 hr is required to produce an FTIR spectrum comparable to the water-rinsed surface. This temperature correlates well with the boiling and decomposition temperatures of boric and phosphoric acids, which are between 135 and 185°C (16). Heating to 50°C under vacuum for 1 hr reduced the FTIR peak area by only 18.2% in the interval from 3750 to 2460 cm^{-1}. Moreover, exposure of a residue-covered BPSG sample at 22°C to a 10^{-8} Torr vacuum for 1 hr produced no apparent change in the FTIR features. Storage of a residue-covered sample in the cleanroom over several days does result in the gradual disappearance of the residue both visually and in the FTIR and generally causes the residue to agglomerate on the surface of the BPSG film.

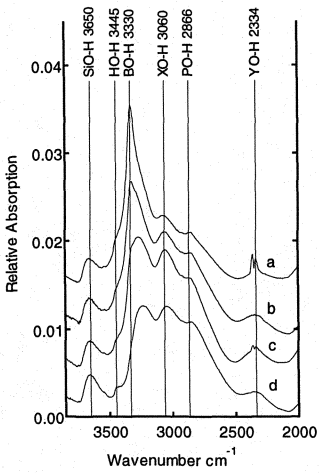

Figure 1: Transmission FTIR spectra after etching 3000 Å of BPSG using AHF at 55°C and 1 atm. Samples were stored in a standard wafer carrier in a class 100 cleanroom at 23°C (a) 10 min, (b) 6 hr, (c) 24 hr, (d) 3 days after etching. A clean Si surface was used as a background for all spectra.

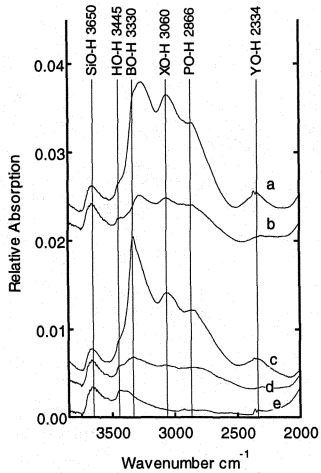

Figure 2: Transmission FTIR spectra after etching 3000 Å of BPSG using AHF at 55°C and 1 atm (a) aged 24 hours, (b) film in a) after exposure to 100°C, 750 mTorr N_2, and direct UV only for 1 hr, (c) aged 2 hrs, (d) film in c) after exposure to 150°C, 750 mTorr 10% Cl_2/90% N_2, and direct UV for 1 hr, (e) ultra pure water rinse for 20 s at 20°C and 760 Torr.

Chlorides of both B and P boil at lower temperatures than the respective acids and the formation of these chlorides is thermodynamically favorable so the mixed acid residue was exposed to atomic chlorine to investigate whether this was a viable removal pathway. Boron trichloride, BCl_3, boils at 12.5°C and phosphoryl chloride, $POCl_3$, boils at 105°C (17). The formation of these chlorides from Cl atoms is thermodynamically favorable at the boiling points

$$B(OH)_3(aq)+3Cl(g)+3e^- = BCl_3(l)+3OH^-(aq) \quad \Delta G^o(293K) = -209\ kJ/mole \qquad (1.1)$$

$$H_3PO_4(l)+3Cl(g)+3e^- = POCl_3(l)+3OH^-(aq) \quad \Delta G^o(373K) = -132\ kJ/mole \qquad (1.2)$$

where ΔG is the change in Gibbs free energy. Exposing dichlorine gas, Cl_2, to UV light from a 1000-watt high pressure Xe arc lamp, formed chlorine atoms. The gas phase photolysis of Cl_2 occurs in the UV in a peak centered at 335 nm (18). Both direct and indirect illumination of the sample surface was tried. Direct exposure to radiation from the lamp heated the surface of the sample to approximately 100°C. The FTIR spectrum in

the O-H stretching region after exposing a residue layer on BPSG aged for 24 hours (Figure 2a) to the UV lamp alone for 1 hr in a N_2 gas flow at 750 mTorr reduced the area of the peaks associated with the B and P-bearing acids by 66.4% (Figure 2b). The shoulder at 3330 cm^{-1} characteristic of the BO-H stretch decreased indicating loss of boric acid. Heating a sample in the cleanroom to 103°C reduced the peak area by 38.8% and heating to 178°C reduced the area by 86.2%, which shows that loss of the residue in the UV only experiment is thermally driven. Heating the reactor walls and adding 10% Cl_2 to the gas phase with direct UV illumination of the sample surface removed more of the residue (89.5%) than in either the vacuum UV only or atmospheric heating experiments (Figure 2d). The residue used was aged for 2 hr (Figure 2c) and the sample surface temperature of 150°C was substantially higher than in the UV only experiment, which may explain the greater removal. The constancy of the BO-H stretch, however, shows that the chemical environment of the boric acid molecules in the residue remained the same, suggesting that there is a component of the removal due to Cl atoms reacting with the acids. The sample surface, however, was covered with an opaque film that could not be rinsed off with water immediately after processing (Figure 4a).

Indirect exposure of a residue to UV-Cl_2 removed a portion of the layer without producing an opaque film. Starting with a residue layer on BPSG that had been stored in a wafer carrier in the cleanroom for 2 days prior to removal, the FTIR spectrum indicated that the 3330 cm^{-1} BO-H stretch shifted to lower frequency (Figure 3a) as described previously due to loss of boric acid and uptake of water (Figure 1). Exposing the 2 day old residue to a gas flow containing 10% Cl_2 and 90% nitrogen at 750 mTorr with the sample oriented parallel to the UV light for 1 hr reduced the FTIR peaks in the O-H stretch region by 38.4% and shifted the boric acid peak to higher frequency indicating that the bond was strengthened, most likely to decreased H-bonding with other components in the residue layer (Figure 3b). The temperature of the sample was 50°C. The sample surface after processing was clear as shown in Figure 4b. A comparable experiment with the reactor walls heated to achieve a sample temperature of 50°C in a pure nitrogen flow at 750 mTorr removed only 18.2% of the residue. Increasing the Cl_2 to a mole fraction of 0.35 reduced the peak area by 47.5%. Rather than due to thermal desorption alone, these results combined with the shift in the BO-H stretch to higher frequency suggest that there is a chemical component to the indirect UV-Cl_2 removal process. Leaving the sample in the cleanroom for 1 day resulted in a further reduction in the O-H stretching peaks without shifting the BO-H stretch (Figure 3c). One interpretation of the data is that Cl atoms react with the acids in the residue to produce volatile products. Further development of this process is required to completely remove the residue layer at low temperatures and to reduce the processing time. A low temperature process is necessary to make residue removal compatible with oxide removal, which is a strong function of temperature (9), so that the two could possibly be integrated into a single reactor and run simultaneously. Preventing the residue layer from forming during the oxide film etch would eliminate sticktion (19) and lead to an all-dry doped oxide removal process.

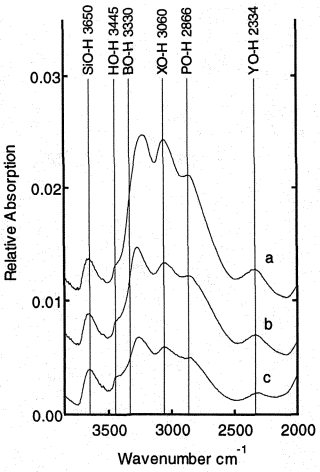

Figure 3: Transmission FTIR spectra after etching 3000 Å of BPSG using AHF at 55°C and 1 atm and storing for 2 days (a) aged residue, compare to Figure 1, (b) after exposure to 50°C, 750 mTorr 10% Cl_2/90% N_2, and indirect UV for 1 hr, (c) storage in wafer carrier in class 100 cleanroom at 23°C and 760 Torr for 1 day after spectrum b was taken.

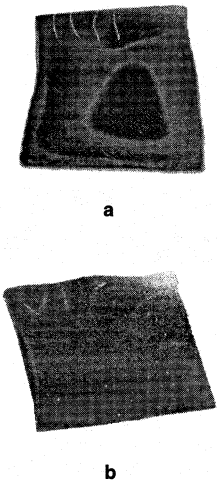

Figure 4: Sample surfaces after 1 hr exposure to (a) direct UV-Cl_2 at 150°C and 750 mTorr (10% Cl_2/90% N_2) and (b) indirect UV-Cl_2 at 50°C and 750 mTorr (10% Cl_2/90% N_2). Scribe marks were made in the upper left hand corner of each sample to distinguish them. The size of the samples is approximately 1.5 cm x 1.5 cm.

HF/Water Vapor Etching of Thermal Silicon Dioxide Films

The removal of SiO and the production of SiF_4 in the gas phase were monitored in real time using FTIR during the etching of a 2000 Å thick thermal oxide film at 40°C and 250 Torr using a gas phase mixture containing a water partial pressure of 17 Torr and HF of 36 Torr. Nine FTIR scans at a resolution of 4 cm^{-1} were co-added every 2 s to obtain the spectra as a function of processing time shown in Figures 5 (750-1200 cm^{-1}) and 6 (3200-4000 cm^{-1}). Time zero is defined as the time that HF entered the reactor. The 17 Torr water vapor partial pressure and 197 Torr nitrogen streams were run for 5 minutes prior to HF entering the reactor. Computer control of the gas handling system allowed HF to be admitted to the reactor without disturbing the total pressure. The spectra at –0.8 s just before HF entered are shown at the bottom of Figures 5 and 6. All FTIR spectra in these figures were backgrounded to a clean Si sample. Gas phase water and HF were also subtracted from each spectrum for clarity. The Si–O stretching vibration at 1080 cm^{-1} decreased and the Si-F vibration at 1026 cm^{-1} increased as a function of time (Figure 5).

The 1080 cm^{-1} Si–O vibration is characteristic of the solid SiO_2 lattice (20) so can be used to monitor etching. The 1026 cm^{-1} is characteristic of the Si-F stretch in gas phase SiF_4 (21). Integrated peak areas for these features are shown in Figure 7. Production of SiF_4 began at approximately 7 s, but SiO_2 did not start etching until approximately 14 s after HF entered the reactor. The delay in etching or induction time is a well known phenomenon in oxide etching and is used to selectively etch oxide films (6-9). The difference in the time for SiF_4 production and the start of etching suggest that even though Si atoms are removed from the surface another process must occur before etching can begin.

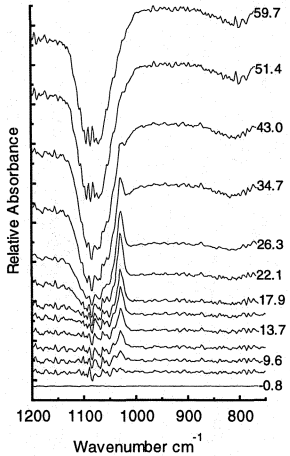

Figure 5: *In situ*, real time transmission FTIR difference spectra in the range 750-1200 cm^{-1} recorded during etching of a 2000 Å thick thermal oxide film at 40°C with 17 Torr of water vapor and 36 Torr HF (250 Torr total p). The time from –0.8 to 59.7 s after HF entered the reactor is shown on the right. All spectra are referenced to a clean Si sample and the FTIR spectrum at zero time. Gas phase water and HF were also subtracted from each spectrum.

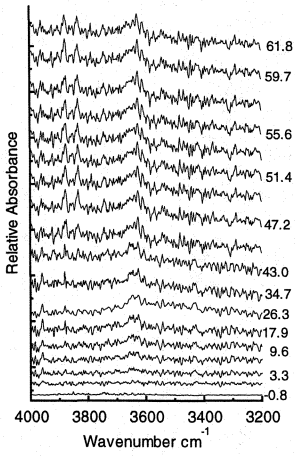

Figure 6: *In situ*, real time transmission FTIR difference spectra in the range 3200-4000 cm^{-1} recorded during etching of a 2000 Å thick thermal oxide film at 40°C with 17 Torr of water vapor and 36 Torr HF (250 Torr total p). The time from –0.8 to 61.8 s after HF entered the reactor is shown on the right. All spectra are referenced to a clean Si sample and the FTIR spectrum at zero time. Gas phase water and HF were also subtracted from each spectrum.

The production of H–bonded silanol groups (SiO–H) occurs as soon as HF enters the reactor. The FTIR difference spectra in the O-H stretching region from 3200 to 4000 cm^{-1} shows a peak at 3650 cm^{-1} that grows continually from the time that HF is introduced into the reactor (Figures 6 and 7). Both the surface of the oxide film and the gas showerhead are probed in this experiment, but the 3650 cm^{-1} vibration is characteristic of silanol groups hydrogen-bonded together (15). Note that these groups are

also present in the doped oxide films described earlier (Figures 1–3) but in that case they were present on both the surface and in the bulk of the oxide layer. With thermal oxide etching these groups are created on the surface by the presence of HF as shown schematically in Figure 8a. HF breaks a siloxane bond fluorinating the Si atom and transferring an H atom to the O forming a silanol group. A majority of the SiO–H groups are H–bonded to one another rather than existing as isolated SiO–H groups, which appear at 3700 cm^{-1} (15). Whether the attack on siloxane bonds by HF is random or activated by the process water requires further study. What is clear from these results is that during the induction period before etching starts silanol groups are created on the surface and, as a consequence, surface Si atoms must be fluorinated. Evidence for Si–F bond formation on the surface is expected at 950 cm^{-1} (21), but the spectra in Figure 5 do not show any features in this range. Even if Si atoms in the first layer, perhaps those that have been hydroxylated before processing, were completely fluorinated to produce SiF_4, which is suggested by the appearance of SiF_4 before etching starts, Si-F bonds are expected on the surface during etching of the bulk oxide film. Previous work showed that F was present on the Si surface after stripping thermal oxides (22).

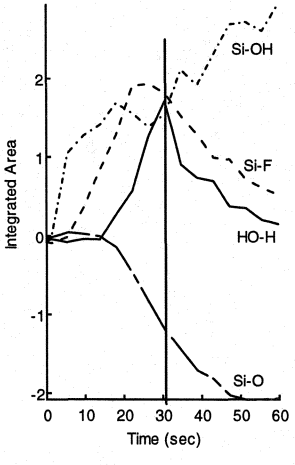

Figure 7: Integrated FTIR peak areas for the 3650 cm^{-1} SiO–H, 1026 cm^{-1} Si-F, 1620 cm^{-1} HO-H, and 1080 cm^{-1} Si–O vibrations as a function of etching time at 40°C and 250 Torr in a mixture of HF and water vapor. The Si–O areas were scaled to 10% of their original values. A total of 2000 Å was stripped.

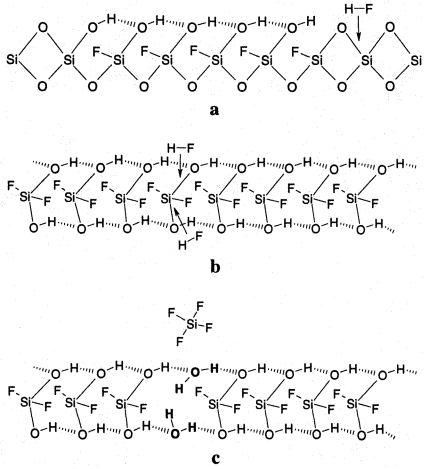

Figure 8: Model HF/vapor gas phase thermal silicon dioxide etching mechanism (a) initiation showing HF unzipping Si–O lattice forming H–bonded silanols, (b) completion of initiation with hydroxylated surface and start of bulk etching regime, (c) production of SiF_4 gas and surface water (center, bold) during bulk etching.

The start of etching coincides with the production of molecular water on the surface. The FTIR difference spectra in the range of molecular water at 1620 cm^{-1} (14) are not shown, but the integrated areas for the 1620 cm^{-1} peak indicate that water production is timed to the start of etching (Figure 7). The 1620 cm^{-1} peak could be water adsorbed on the gas showerhead but would unlikely be timed with the start of etching since the production of water by the reaction is a small addition to the 17 Torr partial pressure already in the reactor due to the water vapor flow. One interpretation of these results and the creation of H–bonded silanol groups on the surface during induction is that each Si atom in the surface region of a patch of the oxide lattice is doubly fluorinated and hydroxylated as shown schematically in Figure 8b. This step completes the induction period. Bulk oxide etching begins when the Si–O bonds in silanol Si–OH are attacked by HF producing water that remains on the surface and liberating a SiF_4 molecule, which desorbs into the gas phase. A schematic of the result of HF attack at the beginning of the bulk oxide etching regime is shown in Figure 8c. Etching is fast since H-bonding with silanol or molecular water weakens the Si–O bonds. Water is continually produced on the surface as etching proceeds and builds up as shown by the increase between approximately 14 and 30 s in Figure 7. At 30 s when approximately one-half of the oxide film has been etched, the etching rate (slope of the integrated Si–O FTIR peak area) achieves a maximum as does the production of molecular water. The production of SiF_4 also peaks near this time. As the etching rate slows down the rate of molecular water decreases and the rate of SiF_4 produced drops. The reason for the etching rate slowing down well before the underlying Si surface is reached is not clear from these results. These conclusions, however, rest on the assumption that the FTIR peak area is linearly related to the oxide thickness, which may not be true. All of the SiO_2 was etched 36 s after the Si–O stretch started to decrease and the molecular water appeared on the surface, which yields a nominal etching rate of 56 Å/s. A recent *ab initio* calculation assumed that the oxide was terminated with geminal silanol groups (two OH groups attached to one Si atom) and showed that HF attack of one of these silanols to fluorinate Si and produce a water molecule was the lowest energy reaction pathway (23). This mechanism is comparable to the bulk oxide etching mechanism proposed in Figures 8b and c. Liquid phase etching mechanisms differ from gas phase mechanisms in the species responsible for etching (24-26). Most studies show a dependence of the etching rate on such species as HF_2^- in solution. One study shows that the replacement of the first O atom by an F ion in liquid phase etching is the rate determining step and subsequent reactions to remove SiF are at least an order of magnitude faster (27), which is similar to the induction time and subsequent bulk etching mechanisms proposed in Figure 8 for gas phase etching.

Further experiments are planned to combine an *in situ* ellipsometer with the FTIR, which will provide real time measurements of the oxide thickness. In addition, a different infrared light path will be added by using attenuated total reflection (ATR) crystals made from Si wafers. The latter addition will probe only the silicon oxide bulk and surface, which will exclude the gas phase and showerhead. Si absorbs in the infrared below 1500 cm^{-1}, however, depending on the path length. The light path in the ATR samples will be

more than 5 cm long, which is enough to hide the Si–O and Si–F features in ATR mode. Future work with real time FTIR will be done using the rapid scan option of the spectrometer, which will improve the signal to noise of interferograms recorded on a much shorter time scale.

CONCLUSION

Removal of the liquid-like residue layer produced by anhydrous HF etching of BPSG films was accomplished without bulk water rinsing using both direct and indirect UV–Cl_2 processes at low pressure and below the boiling and decomposition temperatures of the acids in the layer. The indirect process is the most promising since it could be used to remove residues that are out of the line of sight of the UV lamp owing to mean free paths on the order of 150 μm in the 1 Torr range. Further development is needed with both Cl_2 processes to ensure that the residue can be removed completely and to reduce the processing time. Moreover, other Cl–bearing gases could be used in place of dichlorine that would lead to B and P–bearing products with higher volatilities. The real time FTIR results for low pressure HF/vapor etching of thermal silicon dioxide films suggest that HF hydroxylates siloxane bonds in the surface layer during the induction time fluorinating Si atoms and creating patches of H-bonded silanols, SiO–H. Attack of $SiF_2(OH)_2$ moieties formed during induction by HF produces SiF_4, which is volatile, and molecular water. The attack of the $SiF_2(OH)_2$ moieties, which contain much weaker Si–O bonds than in siloxane, marks the beginning of oxide etching. The film etches at a linear rate until approximately 1000 Å (estimated with the integrated FTIR peak absorbance) is left, when the rate suddenly decreases. Whether this is characteristic of the oxide film or the etching process needs further investigation.

ACKNOWLEDGEMENTS

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VACUUM CLUSTERED DRY CLEANING FOR PRE-GATE SURFACE PREPARATION

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An all dry gas phase pre-gate cleaning process is studied. This process removes light organic contamination, silicon oxide and metal contamination with minimal roughening of the silicon surface. Surface cleaning is achieved through a sequence of ultraviolet illumination, chlorine gas exposure and anhydrous hydrogen fluoride exposure using a hydroxyl-bearing catalyst for silicon oxide removal. Final surface termination may also be controlled by ending with exposure to ultraviolet illumination and oxygen gas. The process is performed in a cross flow vacuum chamber in which the wafer is stationary and both sides can be illuminated and cleaned selectively or simultaneously. Silicon oxide removal with non-uniformity of less than 2% on 200mm wafers has been demonstrated. Removal of trace metal contamination has also been studied and demonstrated while minimizing surface roughening.

INTRODUCTION

As gate dielectric manufacturing progresses towards very thin silicon oxide films and high-k gate dielectrics, it becomes very important to control the silicon surface prior to the gate dielectric step. The surface needs to be clean and free from contamination as well as smooth in order to get the performance needed for 0.1μm technology transistors and beyond. It is also important to transport the surface to the subsequent gate oxidation or deposition step after cleaning as quickly and cleanly as possible to avoid recontamination of the surface. An all dry gas phase pre-gate cleaning module enables both the cleaning and the rapid, controlled transport of the surface by allowing direct clustering with a single wafer deposition system.

Pre-gate cleaning in vacuum-based dry systems has been studied for several years (1,2). However, the extendability of silicon oxide, furnace oxidation and atmospheric aqueous cleaning has delayed the insertion of gas phase dry cleaning into production. It is now clear that the industry is reaching the limit of silicon oxide gate dielectric thickness as it is reduced below 15 angstroms (3-5). While the growth and integrity of silicon oxide gates as thin as 7 angstroms have been demonstrated experimentally, it is likely that below 15 angstroms of equivalent gate oxide thickness (EOT) new materials will be required with dielectric constants greater than 10 (3,4). Several of these materials,

referred to as high-k dielectrics, have already been studied and rejected due to integration difficulties, including tantalum pentoxide and barium strontium titanate (4,5). Materials recently under consideration include zirconium oxide and hafnium oxide (6-8). These materials are also displaying some degree of integration difficulty and will require more study.

Cleaning and surface preparation for these new dielectric materials will be critical. It has been shown that zirconium oxide tends to intermix with silicon at the interface and thus will require a thin barrier (6,7). However, this thin barrier must be tightly controlled so that it does not affect the overall gate capacitance. In addition, it is likely that materials such as zirconium oxide will be deposited by atomic layer deposition methods. Both of these aspects will require a clean and carefully engineered surface for successful integration of the dielectric film.

An all dry gas phase pre-gate cleaning process that removes light organic contamination, silicon oxide and metal contamination with minimal roughening of the silicon surface has been developed and studied. The process chamber and the process will be described. Effectiveness of the cleaning process has been evaluated through thermal oxide etching control, particle performance, metals performance, removal of trace metal contamination, silicon surface smoothness, and final surface termination

PROCESS CHAMBER AND TEMPERATURE CONTROL

A schematic of the vacuum chamber along with gas supplies and vacuum pumps is shown in Figure 1. The process chamber is a simple cross flow configuration with the wafer supported by three pins at the edge. Identical ultraviolet (UV) flash lamps are mounted above and below the chamber and illuminate the top and bottom wafer surfaces through sapphire windows. This configuration allows simultaneous processing of both sides of the wafer. The pulse rate and the discharge voltage are variable and controlled for the UV flash lamps. Process gases are supplied through mass flow controllers (MFC) mounted on a heated gas panel. Nitrogen (N_2), oxygen (O_2) and chlorine (Cl_2) are supplied from standard high purity, high pressure cylinders. Anhydrous hydrogen fluoride (HF) is supplied from a high purity, nickel-plated cylinder which is heated to 30 °C in order to create a cylinder pressure of 7 psig. The oxide etch catalyst is derived from a liquid mixture of isopropanol (IPA: 88%) and water (H_2O: 12%). The catalyst vapor is formed by heating a canister of the liquid mixture to 60 °C and then metering the vapor through a heated MFC. In this work a standard dry vacuum pump with mechanical booster is used, but the system can also be configured with a turbomolecular pump to achieve lower base pressure.

This system takes advantage of the fact that the silicon wafer at near room temperature will absorb UV radiation, while the process chamber absorbs very little. Because of this

characteristic of silicon, the wafer can be heated by the UV lamps and cooling of the chamber is not required, as would be the case with IR heating. In fact the chamber temperature is held at 45 °C by cartridge heaters placed at each of the four corners. This allows the wafer temperature to be determined in two different regimes.

Silicon oxide etching takes place in a low temperature regime. In this regime the wafer temperature must be highly uniform and highly repeatable. To achieve this level of control, the incoming wafer temperature is gently boosted by exposure to 7 seconds of high power UV followed by a 15 second stabilization step. At this point the wafer temperature is regulated by the chamber temperature which is tightly controlled at 45 °C and uniform silicon oxide etching can be achieved.

A high temperature regime is required for efficient treatment with chlorine for metals removal and final surface preparation before gate oxidation. This temperature is typically 100 °C to 200 °C. Although the wafer temperature cannot be directly monitored by non-contact techniques at this levels, the programmed UV exposure is highly repeatable and produces a highly repeatable wafer temperature as measured by a wafer with affixed thermocouples.

PROCESS RESULTS AND DISCUSSION

The pre-gate cleaning process consists of four basic steps. The first step is a pre-conditioning step using UV and Cl_2 during the initial wafer heating ramp. Pre-conditioning is required in order to achieve uniform and repeatable silicon oxide etching. Figure 2 shows a comparison of silicon oxide etch uniformity for 200 angstroms oxide removal with and without the UV/Cl_2 pre-conditioning step. Oxide etching is suppressed at the edges of the wafer due to cassette outgassing and other contaminants on the wafer surface resulting in a non-uniformity of over 16% (standard deviation divided by mean) for a 200mm wafer. Pre-conditioning the oxide surface with UV/Cl_2 reduces the non-uniformity of the oxide etch to less than 1.6%.

The second step is the oxide removal step. Oxide removal is achieved by flowing a mixture of N_2, anhydrous HF and IPA/H_2O vapor catalyst. The temperature of the wafer is allowed to stabilize with the chamber temperature before starting the flow of HF and catalyst vapor. This insures a uniform and repeatable oxide etch. In addition, the incoming gas temperature is controlled to prevent wafer heating or cooling by the flow of process gases over the wafer surface. The total thickness of oxide removed is determined by the exposure time to HF flow. Figure 3 is a plot of oxide removed as a function of HF flow time. The oxide removal rate is very stable at 5 angstroms/second after an initial induction time of 12 seconds.

The third step is a higher temperature step using UV illumination and Cl_2. The wafer temperature is raised about 100 °C by a 15 second exposure to high power UV from the top and bottom lamps. The bottom UV lamp is then turned off and the top UV lamp is turned on at a reduced power level while Cl_2 is flowed over the wafer surface. Figure 4 shows how the silicon surface roughness of epitaxial silicon is affected by exposure to UV and Cl_2. In general, final surface roughness increases as exposure time to UV and Cl_2 increases. However, we have found that silicon doping as well as initial surface roughness play a role in determining final surface roughness. Several different experiments are plotted in Figure 4. In each case, a control wafer from the same lot of silicon wafers was sent for baseline surface roughness measurements. Before and after measurements were not taken on each wafer. Data indicated by the open symbols was collected from wafers of unknown dopant level. Data indicated by the filled symbols was collected from wafers with a better known level of dopant in the epitaxial layer (14-19 ohm-cm, boron doped, 5-7 microns thick). It is believed that the silicon roughness indicated by the open triangle symbols was collected with more highly doped epitaxial silicon. Given the appropriate dopant level, silcon surface roughening can be maintained at less than 1.5 angstroms RMS, with UV/Cl_2 exposures up to 30 seconds. Figure 5 shows the AFM images from the tests indicated by filled circles in Figure 4. In this test, the 30 second process resulted in a surface roughness of 1.5 angstroms RMS. In Figure 5 we can see that darker areas are starting to form at 30 seconds, which are the precursors to pitting seen at longer exposure times.

Ma and co-workers (2) have shown that UV/Cl_2 treatment before gate oxidation produces better gate oxide integrity. The exact reason for the improvement in gate oxide integrity is not understood, but it is believed to be the result of trace metals removal. Previous studies (9,10) have shown the ability of UV/Cl_2 processes to remove high levels of metal contamination. However, those processes tended to leave unacceptable levels of surface roughening. We have attempted to measure metal contaminant removal capability of the low power UV/Cl_2 processes which minimize silicon roughening. At this time we have measured metal contaminant removal for UV/Cl_2 steps as short as 60 seconds. Future work will examine even shorter processes. Achieving repeatable low levels of metal contamination is very difficult. As indicated in Table I, we have had some success with chrome (Cr), nickel (Ni), and Zinc (Zn), achieving challenge levels of less than $1x10^{10}$ atoms/cm^2. We also show data for aluminum (Al) and iron (Fe) in Table I, but were only able to achieve challenge levels as low as $2\text{-}5x10^{11}$ atoms/cm^2. Table I shows that the low power UV/Cl_2 process is effective at removing low levels of Zn and Ni contamination to below detection limit. Even the high levels of Fe contamination were reduced significantly. Mixed results are indicated for Al and Cr and are probably due to variability in the challenge technique (immersion in metal salt solution, followed by spin dry). The process control in Table I also indicates that the process does not add measurable metal contamination to a clean wafer.

The fourth step in the pre-gate cleaning process is optional and may not be required for a fully clustered gate stack system. After UV/Cl_2 treatment, the bare silicon surface is

highly reactive and can easily become contaminated and roughened by exposure to ambient conditions. Therefore, the surface is oxidized by further heating the wafer and then flowing O_2 before removing the wafer from the chamber. Further exposure of the top surface to UV or simultaneous exposure of the top surface to UV and O_2 is avoided for fear of continued etching by adsorbed Cl_2, however this must be studied further. We have found acceptable passivation by continuous heating with the bottom UV lamp while flowing O_2 at 100 torr for 25 seconds. Table II shows measurements of the surface reoxidation by contact angle and spectroscopic ellipsometry for various oxidation processes.

SUMMARY

An all dry gas phase cleaning process has been characterized for pre-gate cleaning. The ability of this process to clean the surface and control the final surface termination at a desired condition may make it applicable to integration with high-k gate dielectric deposition. In addition, the single wafer vacuum chamber can be directly integrated to a single wafer deposition platform so that surface integrity can be maintained during wafer transfer from the cleaning to the deposition chamber.

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Table I. Metals peformance and metals removal. VPD-ICPMS: 10^{10} atoms/cm^2

	Al	Fe	Cr	Ni	Zn
det. limit	0.5	0.1	0.05	0.1	0.2
control	<0.5	<0.1	<0.05	<0.1	<0.2
process control	<0.5	<0.1	<0.05	<0.1	<0.2
challenge	48	24	0.90	0.40	0.40
chal.+60s UVCl	61	9.1	0.06	0.20	<0.2
chal.+90s UVCl	57	4.3	1.0	<0.1	<0.2

Table II. Oxide regrowth processes after native oxide removal

	DI water drop contact angle (degrees)	oxide thickness by ellipsometer (Å)
no O2 process	72.3	6.9
no O2 process	70.8	6.5
both lamps - 30 sec w/O2	41.4	10.2
both lamps - 30 sec w/O2	42.3	9.4
both lamps - 60 sec w/O2	22.3	10.9
both lamps - 120 sec w/O2	24.7	11.4
both lamps - 120 sec w/O2	17.9	10.7
bottom lamp – 120 sec w/O2	20.3	10.0
bottom lamp – 120 sec w/O2	20.2	10.4

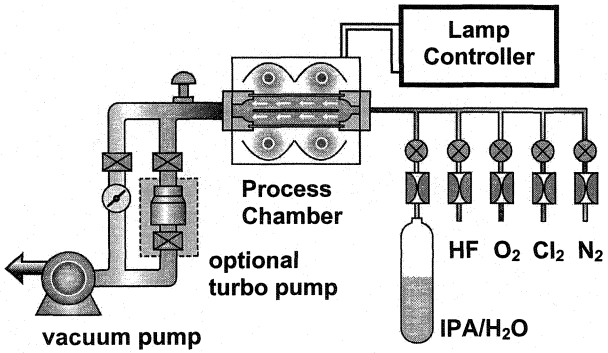
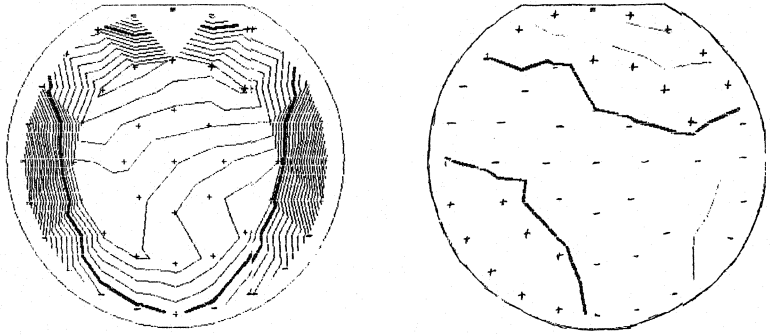


Figure 1. Schematic diagram of vacuum process chamber with gas feeds and vacuum pump.



(a) 16.5%, 1σ

(b) 1.6%, 1σ

Figure 2. Etch uniformity maps for silicon oxide films exposed to anhydrous HF and catalyst. Wafer (a) was processed directly without pretreatment after being held under vacuum in a plastic cassette for several hours. Wafer (b) was also held in the cassette, but received a short UV/Cl_2 pretreatment before the oxide etch.

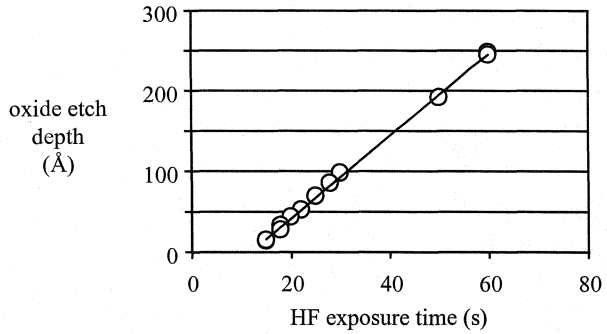


Figure 3. Etch depth of silicon oxide as a function of HF exposure time in an HF/catalyst process.

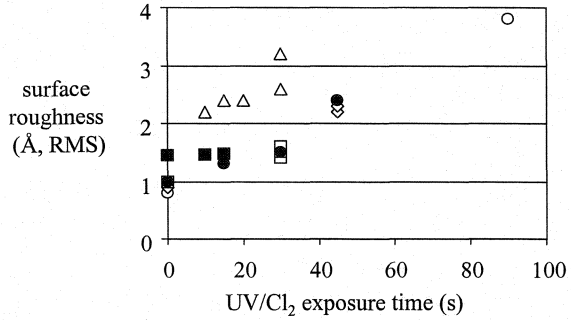


Figure 4. Silicon surface roughness as a function of UV/Cl_2 exposure time. Open symbols represent epitaxial silicon layers of unknown doping levels. Filled symbols represent a known epi resistance of 14-19 ohm-cm, boron.

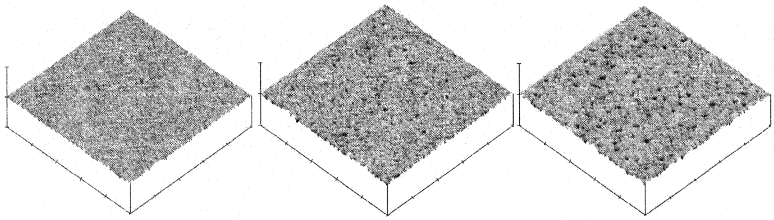


Figure 5. AFM images showing surface roughness of (a) a control wafer with no processing, (b) after 15 seconds UV/Cl_2, and (c) after 30 seconds UV/Cl_2. The precursors to pit formation for this surface are evident after 30 seconds UV/Cl_2.

GAS-PHASE SURFACE CONDITIONING IN A HIGH-k GATE CLUSTER

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This paper introduces a sequence of gas-phase processing steps that is shown to be effective as a treatment applied *in situ* prior to deposition of high-k dielectrics. It produces a chemically clean Si surface which is then subjected to a UV/NO treatment meant to form a film of nitrided oxide about 0.5 nm thick immediately prior to deposition of the high-k dielectric. In this experiment the effect of UV/NO exposure is investigated in conjunction with subsequent mist deposition of $SrTa_2O_6$ films.

INTRODUCTION

Due to the critical role an interfacial oxide plays in a high-k dielectric/silicon gate stack structure the control of the Si surface condition prior to gate dielectric deposition is of fundamental importance. On one hand with the low dielectric constant of SiO_x any interfacial oxide about 1 nm thick or thicker will result in too large a value of equivalent oxide thickness (EOT) defeating the purpose of introducing the alternative dielectric featuring a higher dielectric constant k. On the other hand, however, a thin interfacial oxide may be needed to reduce the interface trap density and by smoothing the transition from single-crystal Si to the amorphous high-k gate dielectric to improve electron mobility in the channel of the MOSFET. It has been postulated [1] that an interfacial oxide of about 0.5 nm should be enough to meet these requirements. In addition, it is highly desirable that the interfacial oxide be nitrided to increase its dielectric constant and also to minimize possible boron penetration of the oxide from p-type poly-Si gate contacts as well as additional oxidation of silicon during high-k dielectric deposition.

It is postulated that such precise control of the interfacial oxide can be best achieved by means of gas-phase surface treatments. The use of gas-phase chemistries for pre-processing of Si surfaces was considered a long time ago [2] and specific recipes for pre-gate oxidation surface cleans were explored (e.g.[3-6]). However, in spite of their mostly adequate performance none of them was adopted into mainstream batch manufacturing mainly due to the continued improvement of wet cleaning technology in light of which any drastic changes of manufacturing procedures were not warranted. It appears, however, that in the specific case of Si surface treatments prior to deposition of high-k gate dielectrics, dry surface treatments are better suited than their wet counterparts to address emerging challenges.

It is important to stress that any sequence preparing Si surfaces for high-k deposition should start with *ex situ* wet cleaned Si wafers free from particles and metallic contaminants. The subsequent gas-phase surface conditioning sequence should be integrated with a high-k deposition step in an adequately configured cluster tool. In the sequence explored in this study the native/chemical oxide is removed first. This step can be implemented using a well-established AHF/methanol process (e.g. [7]). Then, chemical residues remaining on the surface, specifically fluorine, should be removed. Due to the strength of the Si-F bond the most effective technique may be slight etching of the Si surface which can be accomplished by exposing the Si surface to UV/Cl_2 irradiation [8]. This particular process was evaluated for pre-gate oxidation applications [5,9] and, if properly performed, is expected to produce a chemically clean, smooth Si surface [10]. At this point the Si surface is considered to be ready for the regrowth of the 0.5 nm thick nitrided silicon oxide. In this experiment this process is implemented by UV/NO exposure at temperatures of 200 °C or lower. The feasibility of this process was originally demonstrated at 500 °C [11] which is too high to assure controlled growth of an oxide in the thickness regime from 0.5 to 1.0 nm. The NO was selected over N_2O for its better ability to passivate interface states [12].

In this experiment the proposed method of gas-phase Si surface conditioning is investigated as an integrated process implemented in a commercial cluster prior to high-k gate dielectric deposition. It is postulated that by incorporating a complete surface preparation sequence into high-k dielectric gate stack manufacturing the resulting process may allow better control of interface characteristics than approaches considered earlier (e.g. [13]). The use of the photo-stimulation of the NO oxidation process may also allow control of nitrided oxide thickness below 1.0 nm which is very difficult to accomplish using elevated temperature NO or N_2O oxidations (e.g.[14]).

EXPERIMENTAL

150 mm and 200 mm, p-type, (100), prime Si wafers were used in this study. The experiments were performed using a commercial cluster tool [15] consisting of a 200 mm compatible gas-phase surface conditioning module, a Liquid Source Misted Chemical Deposition (LSMCD) module and a low-temperature RTP module (Fig. 1). The surface conditioning module is equipped with UV/O_2, anhydrous HF/methanol, UV/Cl_2 and UV/NO capabilities and was described in detail earlier (e.g. [5,7]). The module uses a broadband Xenon lamp to generate UV radiation and IR lamps to heat the wafer.

Following completion of the gas-phase surface conditioning sequence, the wafers are transferred via an ultra-pure nitrogen filled central module to the high-k dielectric deposition module (Fig.1a). The deposition is carried out by means of the LSMCD method [15] which uses liquid metal organic precursors and deposits a controlled amount of liquid onto the surface in the form of a fine mist (Fig.1b). Following mist deposition wafers are transferred to a low temperature rapid thermal process module for annealing.

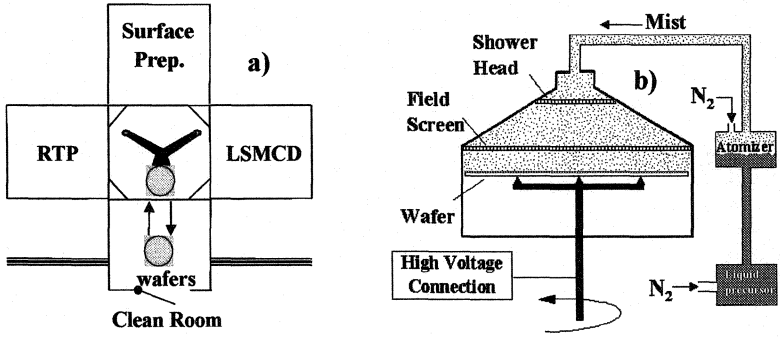

Fig. 1 Schematic diagram of (a) cluster tool and (b) LSMCD module.

The annealing sequence includes low-temperature steps at 160 °C and 240 °C in oxygen and a brief 700 °C anneal in either oxygen or nitrogen.

The high-k dielectric used in this study was $SrTa_2O_6$. This particular material was selected for its good coverage of hydrophilic surfaces during mist deposition, as well as its expected limited thermal stability resulting in the release of oxygen atoms which can then grow interfacial oxide at the Si-high-k dielectric interface. The degree to which the growth of an interfacial oxide can be prevented by the interfacial oxide formed using the sequence ending with UV/NO exposure is used as a measure of its effectiveness. Material characterization was carried out in this study using Transmission Electron Microscopy (TEM), X-ray Photoelectron Spectroscopy (XPS) and Atomic Force Microscopy (AFM). Thicknesses of the oxide stacks were determined by means of ellipsometry as well as cross-sectional TEM. In addition, Pt or Pt/Ti-gate MOS capacitors were formed on processed wafers and conventional C-V and J_g-V characterization was carried out to determine key electrical characteristics of the gate stacks investigated.

RESULTS AND DISCUSSION

It was demonstrated that the AHF/methanol oxide etching process is very sensitive to the starting condition of the etched oxide [16,17], and hence, it is appropriate to verify its kinetics for any given set of experimental conditions. In this experiment the process was qualified by etching thermal oxides on wafers stored in closed containers in a clean room ambient. Figure 2 shows the results obtained which were found in agreement with results obtained earlier using a different module from the same manufacturer [7]. For the next stage of this experiment a wafer temperature of 45 °C and ambient pressure of 150 torr was selected for the AHF/methanol oxide etching step. A similar process qualification was performed in the case of the subsequent UV/Cl_2 irradiation. Here, the

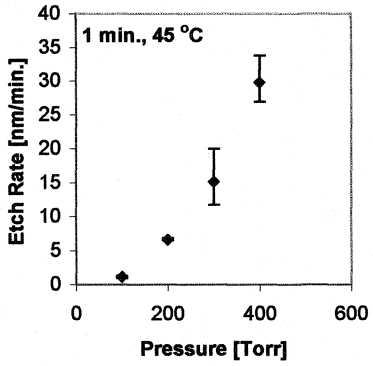

Fig. 2 Oxide etch rate of AHF/methanol step.

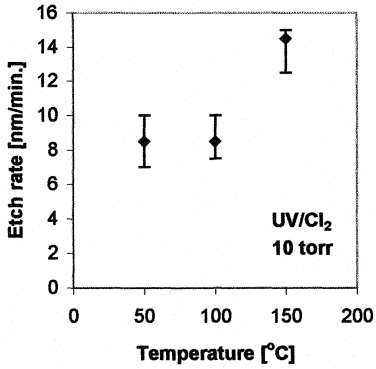

Fig. 3 Si etch rate of UV/Cl_2 step.

thickness of Si etched during UV/Cl_2 exposure following AHF/methanol treatment was used as a measure of process performance. As shown in Fig. 3 a few nm of Si can be removed during a short exposure at temperatures between 50 and 100 °C. The wafer temperature of 75 °C and pressure of 10 torr were selected as parameters of the UV/Cl_2 process in pre-gate dielectric deposition surface treatments used later in this study. The mechanics of UV/Cl_2 Si etching are suggested to be such that Cl attacks the Si-Si back bond and removes residual F from the surface as $SiCl_3F$. Hence, an assertion is being made that the Si surface at this point is mostly free of any chemical residues, including chlorine, although we don't have direct evidence to support this contention. Indirect support was provided by SIMS depth profiling across a Si epi layer and its interface with a substrate exposed prior to epi growth to an AHF/methanol + UV/Cl_2 sequence. The results of this characterization did not show Cl present at the epi-substrate interface [10].

In the next part of this investigation the kinetics of UV/NO oxidation were studied. Wafers prior to UV/NO exposure were *in situ* subjected to AHF/methanol and UV/Cl_2 steps applied in sequence. As shown in Fig. 4 UV/NO exposure at 10 torr without any wafer heating results in the formation of an oxide about 1 nm thick as determined by standard ellipsometric measurements. Oxide thickness is increased to about 1.3 nm when the wafer temperature during UV/NO exposure is increased to 200 °C. It is understood that standard ellipsometric measurements of ultra-thin oxides may not give an accurate estimate of the oxide thickness particularly when its composition is likely to be somewhat different from stoichiometric SiO_2. To address this uncertainty wafers processed in the cluster with the sequence ending with UV/NO exposure were evaluated by XPS. Table 1 summarizes the results of XPS characterization. As seen in the table the process without any IR heating results in an effective oxygen coverage amounting to less than 0.1 nm of

mean oxide thickness with no detectable nitrogen content. This indicates that without any thermal enhancement the UV/NO process effectively is not growing any coherent oxide

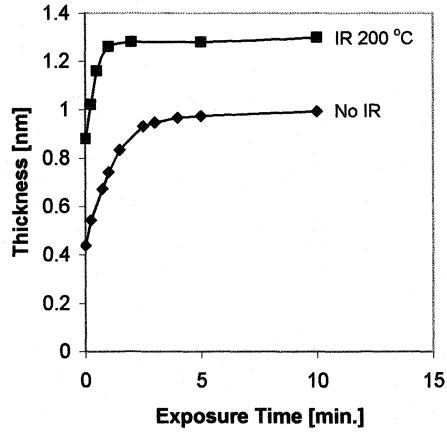

Fig. 4 Kinetics of UV/NO oxidation.

film on the surface in spite of the fact that ellipsometric measurements may indicate otherwise. However, when the wafer temperature during the UV/NO exposure is increased to 200 °C, formation of an oxide about 0.5 nm thick with nitrogen atomic concentration over 2% was determined by XPS (Table 1). Considering that the XPS measurement is carried out in high vacuum which removes species weakly adsorbed on the surface while ellipsometric measurements are carried out in an air ambient the former is considered to produce a more accurate picture of the chemical condition of the Si surface following UV/NO exposure. While the XPS determined thickness of the oxide is ideal for the oxide to act as an interfacial oxide in a high-k dielectric gate stack the nitrogen content in the oxide may not be sufficient to provide an effective barrier against uncontrolled additional oxidation of the Si surface during high-k dielectric deposition. The nitrogen content can be increased by increasing wafer temperature and/or process pressure during UV/NO exposure but any such modification will invariably result in an undesired increase of the oxide thickness.

In order to evaluate the effectiveness of the discussed procedure in high-k dielectric gate oxide formation the next step in this investigation was the integration of the introduced above surface conditioning sequence with mist deposition of $SrTa_2O_6$. Because wafer transfer from the surface preparation module to the mist deposition module (Fig.1a) takes place in the cluster in ultra-high purity nitrogen it was expected that the chemical condition of the Si surface is not altered during the wafer transfer. In earlier experiments with $SrTa_2O_6$ mist deposited on *ex situ* HF-last treated surfaces an interfacial oxide of thickness in the range of 2.5 nm was consistently observed using

Table 1. XPS measurements for UV/NO processes.

	Relative Conc. (Atom %)				
Process	Si	C	O	N	XPS Thick. (nm)
UV/O2	62.3	10.5	21.7	0.0	0.2
UV/NO (No IR)	60.6	7.4	30.9	0.0	0.2
UV/NO (IR 200 °C)	54.2	18.5	25.0	2.3	0.5

cross-sectional TEM characterization (Fig. 5). In an attempt to determine what step of the process is mainly responsible for the growth of this oxide various post-deposition thermal treatments ending with a brief treatment at 700 °C in either oxygen or nitrogen were considered. Invariably the same interfacial oxide resulted indicating that the Si at the interface becomes oxidized by oxygen from the $SrTa_2O_6$ during the 700 °C step. Capacitance-voltage (C-V) measurements at 1 MHz (Fig.6a) did confirm an EOT value similar to the thickness of the interfacial oxide revealed by TEM. This provided a good situation to test the effectiveness of the pre-deposition sequence involving UV/NO exposure. If it is successful in blocking oxidation of the Si and decreasing thickness of an interfacial oxide then reduction of the EOT should be observed.

Following the above reasoning, the next step in this experiment was deposition of $SrTa_2O_6$ carried out under the exact same conditions as earlier, but on Si surfaces which were *in situ* subjected to the full surface conditioning sequence described above. As shown in Fig. 6a, the MOS capacitors obtained in this way display higher capacitance in accumulation which, under the conditions of this particular experiment is an indication of reduced EOT (1.4 nm as compare to 1.8 nm for the HF-last surface). Furthermore, the leakage current across the gate stack was reduced (Fig. 6b) when the UV/NO step was incorporated into the process. As the total thickness of the gate oxide stack did not change significantly the changes observed are likely due to the different band alignment suggesting a composition of the interfacial oxide possibly different than in the previous case.

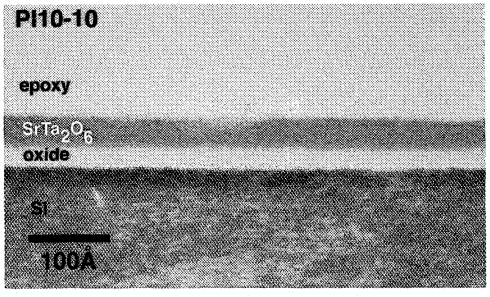

Fig. 5 TEM cross-sectional picture of $SrTa_2O_6$ film deposited on HF-last surface.

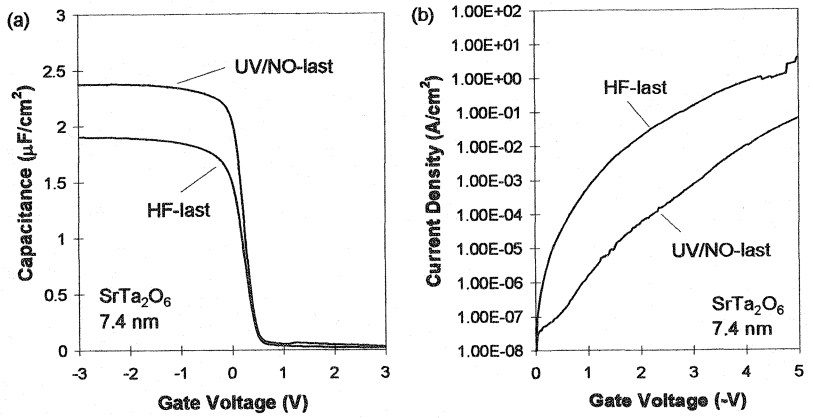

Fig. 6 (a) C-V and (b) I-V characteristics of $SrTa_2O_6$ MOS capacitors on HF-last and UV/NO-last treated surfaces.

SUMMARY

The results of this investigation indicate that the surface conditioning treatments explored in this study may be a right step on the way to finding solutions to the problems associated with alternate high-k dielectric/Si interfaces. The concern is a relatively low concentration of nitrogen in the interfacial oxide. Still, experimental evidence obtained in this study shows that the pre-deposition surface treatment employed results in improvements in EOT as well as leakage current of the high-k dielectric MOS gate stacks.

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ETCHING OF SILICON NATIVE OXIDE USING ULTRA-SLOW MULTICHARGED Ar^{q+} IONS

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Etching of native silicon oxide on the silicon surface using ultra-slow multicharged Ar^{q+} (q>1) ions is investigated. As opposed to "kinetic sputtering" using singly charged argon ions (Ar^{1+}) oxide removal using multicharged ions is accomplished primarily by a "potential sputtering" mechanism. The ion dose needed to obtain complete oxide removal for different ion charge state is determined. It is demonstrated that by using ultra-slow multicharged Ar^{q+} ions instead of singly charged ions with higher kinetic energy native oxide can be removed essentially without any damage to the Si surface and sub-surface region.

INTRODUCTION

Removal of native/chemical oxide is a key step in the conditioning of silicon surfaces in a variety of processes in silicon device manufacturing. Several methods of native oxide etching are available. Wet etching using dilute HF has been in use for many years in this application, but the trend toward process integration calls for improved methods of native oxide control using gas-phase processing. Each of the currently available dry methods of native oxide etching has some limitations. Purely chemical methods, such as anhydrous HF/methanol processes may leave excess fluorine on the surface [1] while purely physical methods, such as ion sputtering using single-charge Ar^{1+} ions tend to damage the surface as certain minimum kinetic energy of impinging ions is needed to sputter off an oxide [2]. The hydrogen reduction process on the other hand requires a temperature of 900 °C to be effective which renders it incompatible with low-temperature epitaxial deposition processes. In the case of remote plasma H_2 reduction pitting of Si surface during oxide etching may be a problem.

In this study etching of native silicon oxide using multicharged argon ions (Ar^{q+}, q>1) with a kinetic energy in the order of a few eV/q is explored. In contrast to singly charged ions, Ar^{1+}, the interaction of slow multicharged or highly charged ions (MCI or HCI) with a surface is dominated not by the ion's kinetic energy, but by its potential

energy, i.e. the energy needed to excite atom from the ground state to the ionized state. Depending on the charge state the potential energy of the ion can vary from tens to hundreds of eV and can even be as high as few keV for highly ionized atoms. The way this potential energy is released over the solid surface is related to a new type of sputtering, or desorption process referred to as "potential sputtering"[3]. By using ultra-slow multicharged ions with high potential energy instead of singly charged ions which require certain minimum kinetic energy to etch the oxide, the effectiveness of ion beam etching can be extended to the kinetic energy regime below 30 to 40 eV. Studies of the various processes and phenomena involved in "potential sputtering" along with more fundamental aspects are discussed in details elsewhere [4] and other applications beside etching are currently under development [5].

The purpose of this investigation was to study etching on native oxide spontaneously grown on Si surface oxide using multicharged argon ions (Ar^{q+}, $q>1$). Included in this investigation is a thorough analysis of Si surface following etching with singly charged and multicharged Ar ions.

EXPERIMENTAL

In this experiment wafers were irradiated in the X-ion's commercial PEXS-1 eV system (Fig.1). The strong magnetic confinement of Electron Cyclotron Resonance (ECR) ion source combined with a high frequency RF heating make it very efficient in producing multicharged ions. Currents obtained range from μA to mA depending on the desired charge state. In this experiment multicharged argon ions (Ar^{q+}, $q>1$) were produced with a SuperNanogan ECR ion source powered by a 14.5 GHz klystron. Charge states up to Ar^{11+} were used. After extraction and charge selection with a bending magnet , the ions were directed toward the silicon substrate. Before reaching the wafer, ions are decelerated to a kinetic energy close to 1 eV/q via a deceleration platform (Fig. 1). Ion beam monitoring is done with an *in situ* beam imaging technique [6]. Singly charged ions were also extracted from the same ECR ion source and were used at a kinetic energy of 1 keV. All irradiation were carried out with the ion beam impinging normally on the surface and at room temperature. The base pressure of 10^{-9} torr is maintained in the process chamber.

The Si wafers subjected to MCI irradiation in this experiment were 100 mm, (100), p-type, directly "out of the box " i.e. as received from the manufacturer. Before and after irradiation wafer surface was analyzed using an *in situ* Auger Electron Spectroscope (AES) (Fig. 1). After samples were removed from the MCI reactor wafer surface was further characterized using Atomic Force Microscope (AFM) and Spectroscopic Ellipsometry (SE) . In addition, electrical characterization of etched surfaces was carried out by measuring electrical characteristics of thermally evaporated, 1 mm in diameter Al-gate MOS capacitors formed on irradiated surfaces. The gate oxides were thermally grown at 900 ^{o}C in O_2 to the thickness of about 12 nm.

RESULTS AND DISCUSSION

The Auger spectra obtained in this experiment are presented in Fig. 2. The spectra show the derivative of the LVV silicon Auger lines. Considering the inelastic mean free path for electrons of a few hundreds eV of kinetic energy , the spectra represent only the first few atomic layers. A clear peak originating from the oxidized silicon and seen around 75 eV was observed before irradiation. This peak is gradually replaced during the irradiation by a silicon-silicon peak at 92 eV indicating a gradual removal of the silicon oxide layer. In this study the complete disappearance of oxidized silicon peaks was taken as a measure of a full oxide removal.

The next point of interest in this investigation was the determination of the ion dose needed to accomplish complete etching of native oxide using ions featuring different charge state. With singly charged ions, the dose necessary to etch off the native silicon oxide is mainly a function of the kinetic energy of the ion and to a lesser extent of the ion species and the angle of incidence [7]. For kinetic energy below 30 to 40 eV it usually ranges from 10^{17} ion/cm^2 to 10^{19} ion /cm^2 . In the case of multicharged ions we found that the dose depends mainly on the ion charge state (Fig. 3). Specifically, it was determined that the ion dose needed to remove the oxide layer decreases while increasing the ion charge. The lowest dose of about $3x10^{15}$ ion/cm^2 was found for Ar^{11+} ions which was the highest charge state used in that study. It has to be noted that singly charged ions can also etch oxide at such low doses, however, they can only do it at the kinetic energy in the range of 1 keV. In the case of Ar^{1+}, ions are damaging the surface even if they are impinging on the surface at the glancing angle [8].

In order to evaluate surface damage incurred during oxide etching the AFM images of the surface were taken before and after irradiation. As images in Fig. 4 illustrate, an increase of the surface roughness of 0.05 nm rms was observed following MCI irradiation. This result was reproduced for Si(111) wafers as well as for Si(100) epitaxial wafers. Though this increase is not negligible it is considered to be significantly lower than the one expected in the case of irradiation with high kinetic energy Ar^{1+} ions.

In addition to AFM measurements, spectroscopic ellipsometry was used to evaluate surface damage. Although qualitative in nature, the SE characterization allows direct monitoring of the variation of the pseudo-dielectric function which provides physically meaningful information regarding condition of the Si surface. Figure 5 a/ illustrates changes of the imaginary part of the pseudo-dielectric function ($<\varepsilon_2>$) for Ar ions with different charge states at the irradiation dose selected to accomplish complete removal of native oxide. As a reference, readings from the dHF (1% HF, 1min dip) etched Si surface are used. Consistent with an observation that a lower ion dose is needed to etch off the native silicon oxide layer when increasing the ion charge state (Fig.3), the departure from the reference curve decreases when increasing the ion charge indicating a less damaged surface. The results from Ar^{1+} irradiation are also shown in Fig.5 a/. A much more

pronounced departure of the dielectric function from the one of the reference surface is observed in this case. Not only the maximum of the 4.3 eV peak is significantly reduced, but also a global shift toward lower energy, characteristic of at least partial surface amorphization is depicted in Fig.5.

In order to better understand the nature of surface damage inflicted by ion interactions, a vacuum anneal at 600 ^{0}C for 30 min. was performed after irradiation and subsequently the SE spectra were taken again. As Fig.5 b/ illustrates only minor improvement is observed for Ar^{1+} irradiated surface following an anneal. In the case of Ar^{11+} irradiation, however, the same anneal results in almost complete recovery of the irradiated Si surface. These results indicate different nature of the Si surface damage in the case of singly charged and multicharged ions. In the latter case, a reversible displacement of the Si atoms from their original lattice sites may be taking place. In the former case, however, mostly irreversible change in the structure of the Si surface is observed.

In the last part of this experiment the electrical characterization of the MOS test structures formed on the Si surfaces from which native oxide was etched using singly charge and multicharged ions was carried out. The typical current density vs. electric field, J-E, characteristics of MOS capacitors in the case of etching with fully decelerated Ar^{11+} ion beam and 1 keV Ar^{1+} ion beam are shown in Fig.6. A distinct difference in the shape of the plots shown can be observed. First, a catastrophic oxide breakdown is taking place at the lower electric field of about 3 MV/cm in the case of "kinetic sputtering" using singly charged ions. Second, in contrast to singly charge ions etching, oxides formed following MCI "potential sputtering" display a distinct signature of the Fowler-Nordheim tunneling across the oxide before its catastrophic, irreversible breakdown takes place (Fig.6). The latter behavior is expected for the MOS structures with oxides in the 10-12 nm thickness regime indicating that the Si surface before thermal oxidation was not altered by MCI etching in any major way. In contrast, the Si surface subjected to Ar^{1+} "kinetic sputtering" sustained a damaged which did not allow formation of the gate oxide displaying adequate electrical integrity. These results further underscore a significant difference in the nature of interactions with Si surfaces between singly charged and multicharged ions.

SUMMARY

The use of ultra-slow multicharged ions for the purpose of native oxide etching has been investigated. It was demonstrated that the native silicon oxide can be sputtered off the Si surface using multicharged Ar ions (Ar^{q+}, $q>1$) with significantly less surface damage then in the case of singly charged argon ions Ar^{1+} etching. It was found that not only the extend, but also the nature of the damage of the Si surface in these two cases is very different. These results exemplify the difference between "potential sputtering" and "kinetic sputtering" implemented using multicharged and singly charge Ar ions

respectively. Using the former, a physical etching of a native oxide can be accomplished with almost no damage to the Si surface.

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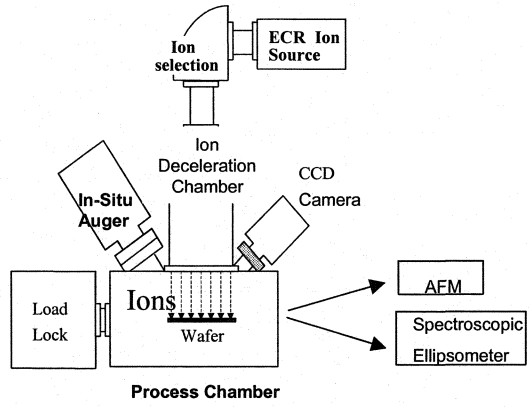

Fig. 1. Experimental set-up used in this study

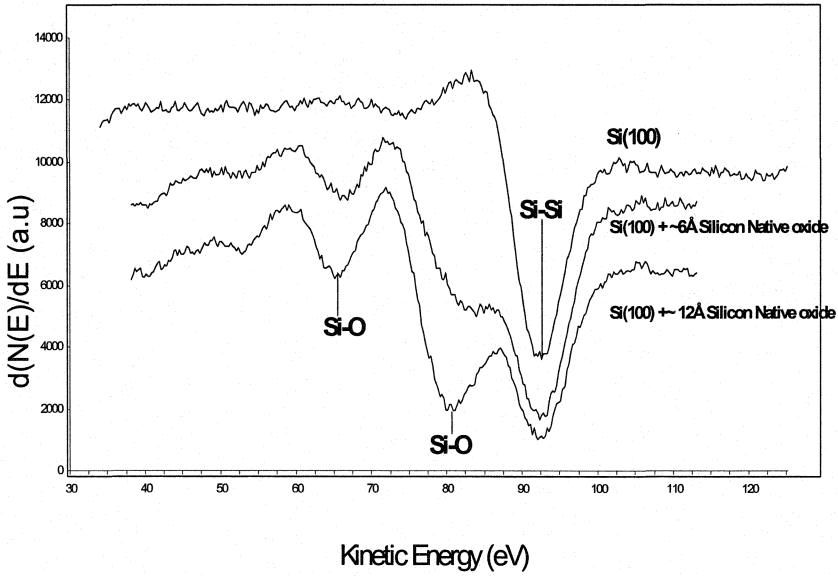

Fig. 2. Auger spectra showing native silicon oxide removal using ultra-slow Ar^{11+} ions : before processing (bottom), half removed (middle) and completely removed (top).

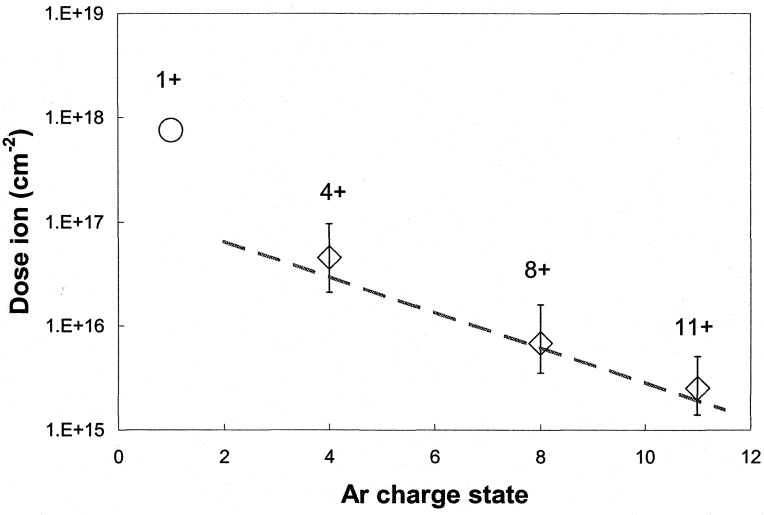

Fig. 3. Ion dose (Ar^{q+}/cm^2) needed to remove the silicon native oxide layer versus ion charge state.

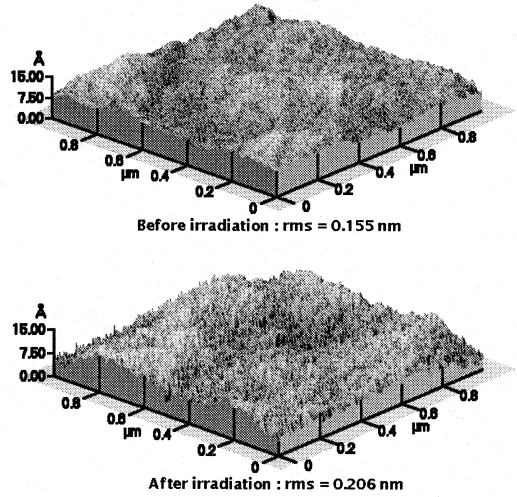

Fig. 4. AFM pictures of Si surface before and after irradiation with Ar^{11+} resulting in the removal of native oxide.

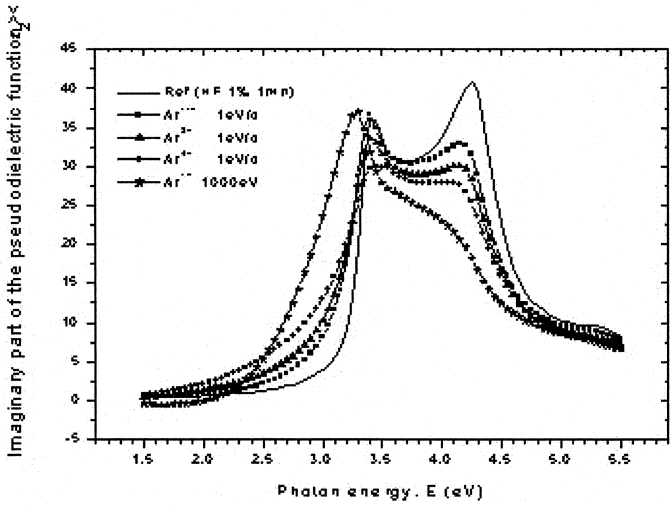

Fig. 5a Modification of the imaginary part of the pseudo-dielectric ($<\varepsilon_2>$) function after irradiation with various Ar charge state (Ar^{1+}, Ar^{4+}, Ar^{8+} and Ar^{11+}) with respect to a HF treated surface.

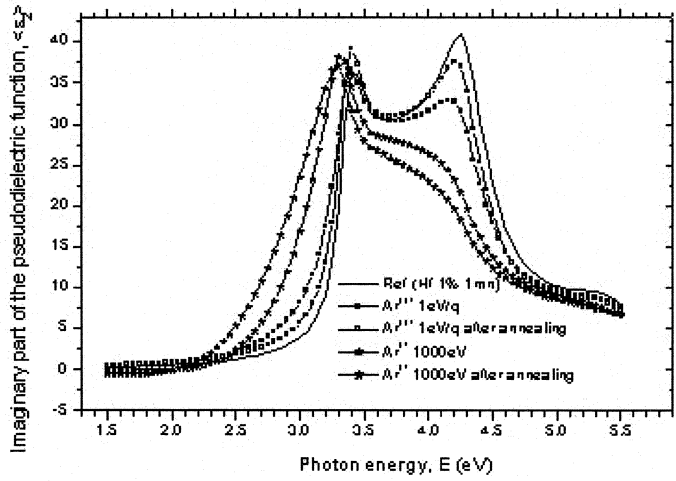

Fig. 5b Effect of a 600 °C anneal on the pseudo-dielectric function for the recovery of the etched surface irradiated with Ar^{11+} at 1eV/q kinetic energy and Ar^{1+} at 1 keV.

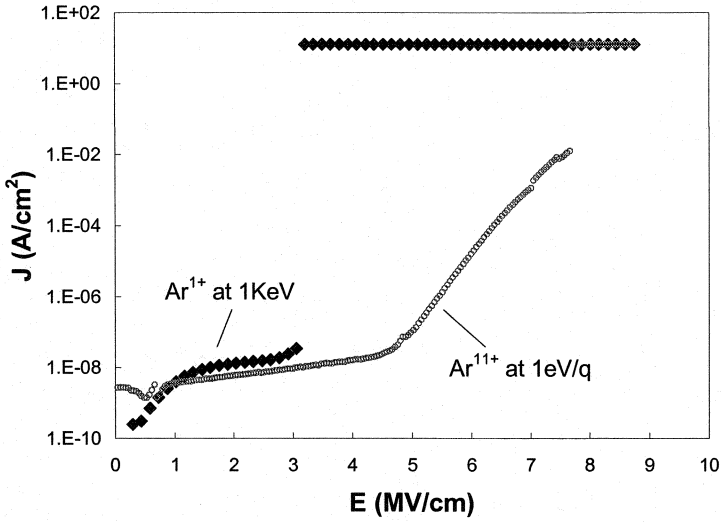

Fig. 6 Current density - electric field characteristics showing typical breakdown characteristics of oxides grown on Ar^{1+} and Ar^{11+} irradiated Si surface.

CRYOKINETIC CLEANING ON CU/LOW-K DUAL DAMASCENE STRUCTURES

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Particle removal with a cryogenic aerosol of argon and nitrogen has been successfully implemented in the fabrication of integrated circuits with copper dual damascene interconnects. Cryogenic aerosol is particularly useful with copper and low-k dielectrics because it achieves efficient particle removal while avoiding many of the problems of traditional liquid chemical cleans. We have demonstrated the cleaning efficiency of cryogenic aerosol on polished surfaces and surfaces with open vias. The process has been shown to have no effect on low-k films, through FTIR spectra and ellipsometry measurements, while maintaining film integrity. Low-k, very low-k, and ultra low-k (porous) films have been investigated.

INTRODUCTION

When cleaning wafers that use Cu dual damascene interconnects with low-k dielectrics, a whole host of problems can be encountered. These include the standard Back End of Line (BEOL) cleaning problems of low cleaning efficiency and excessive etch rates leading to shifts in critical dimensions and metal corrosion. In addition, one must deal with shifts in dielectric constant, compatibility with Cu, corner rounding, collapsing trench walls, film delamination, and Photo diode Induced Copper Redeposition (PICR) (1,2). One clean that avoids all these pitfalls, is the Ar/N_2 cryogenic aerosol (CryoKinetic) clean. In those instances where particle cleaning is the main issue, wet chemistries, and their inherent issues with Cu and low-k dielectrics, can be avoided by using CryoKinetic cleaning.

Copper dual damascene can be implemented many ways. The four most common integration schemes are labeled Self-Aligned, Partial (or half) Via First, Via (or Full) First, and Trench First. Of these, the most common are Partial or Full Via First. All of these schemes utilize a stack with a Via Etch Stop that doubles as a Cu diffusion barrier and some sort of ILD/IMD stack. Within this ILD/IMD stack there may or may not be a Trench etch stop and a top Hardmask layer. Each of these potential changes to the

integration scheme have implications on what constitutes the best cleans process. In all cases, there are at least four cleans (Figure1) and as many as six cleans required to complete one interconnect level with associated Vias. Cleaning opportunities include post CMP (Cu and possibly ILD polish), Pre-ILD, Pre-IMD, post Via, post Trench, post Etch stop, and pre-PVD. Each of these opportunities may be a single or a multi-step clean sequence. CryoKinetic cleans can be used at both post Via (Fig. 1a) and pre-ILD (Fig 1d) clean steps.

Typical removable defects on the wafer surface before ILD deposition are shown in Figure 2. Defects can range in size from several microns (Figure 2a) to only a few hundred nanometers (Figure 2b). These defects originate from the polishing process, transport cassettes, and general handling. There are some defects that are not cleanable or repairable with CryoKinetic cleaning. These defects are shown in Figure 3 and include dried slurry residue and scratches or ripouts. In as much as ripouts are often caused by particles that were left on the wafer at a previous level, CryoKinetic cleaning will help reduce ripouts by preventing them in the first place.

CryoKinetic cleaning efficiency has been demonstrated on polished surfaces and surfaces with open vias. The process has also been shown to have no effect on low-k films through FTIR spectra and dielectric constant measurements, while maintaining film integrity. In previous studies CryoKinetic cleaning has been shown to be non-damaging and non-charging to the wafer surface (3). Defect removal and yield improvement using this process for Al/TEOS BEOL has also been previously reported (4).

CRYOKINETIC CLEANING

CryoKinetic cleaning was introduced to IC wafer manufacturers in 1996. In CryoKinetic cleaning, the wafer surface is cleaned by an aerosol of microscopic argon/nitrogen ice crystals in a nonchemical, nondamaging process (3,5). A mixture of argon and nitrogen gases at approximately 70 psi is cooled to form a liquid/gas mixture. This mixture flows into a tube and is injected through small holes into the vacuum chamber. The flow is directed toward the wafer surface. As the liquid/gas mixture is injected into the vacuum chamber, the liquid portion expands and breaks up into small fragments. The fragments undergo evaporative cooling causing them to freeze into solid crystals which range in size from under 0.5 μm to over 5 μm and which can attain velocities of up to 100 m/s.

Contaminants are dislodged from the wafer surface mainly through momentum transfer from the ice crystal to the contaminant particle. Once dislodged, the contaminant particle is carried away from the surface of the wafer by thermophoretic and convective forces and is swept out of the cleaning chamber by a carefully engineered laminar flow field (6,7). Contaminant particles and ice crystals are carried into the exhaust where the ice crystals simply undergo sublimation back to gas-phase argon and nitrogen.

CLEANING EFFICIENCY

The cleaning efficiency of the CryoKinetic process has been demonstrated on a number of particles and surfaces. Figure 4 shows the cleaning efficiency on 300mm wafers for silicon nitride particles greater than 0.09 micron on a bare silicon surface. The starting challenge count was approximately 5000 at 0.09 micron and above, and the CryoKinetic process removed over 98% of those defects. Cleaning efficiency has also been measured on other surfaces. Butterbaugh and co-workers have shown over 99% removal of oxide particles from an oxide patterned tungsten silicide wafer and over 99% removal of broken wafer particles from a metal patterned wafer (8)

CryoKinetic cleaning is also effective at removing many defects that are generated during the Cu dual damascene processing sequence. As previously discussed, Figure 2 shows typical defects on the surface of the intermetal dielectric (IMD) following copper damascene polishing and cleaning. These defects are easily removed with the CryoKinetic process. Removal of these and many other types of defects significantly improves electrical yields in the Cu/Low-k dual damascene integrated process. Figure 5 compares cleaning efficiency and particle additions for various pre-ILD cleans. CryoKinetic cleaning matches the removal efficiency of the best wet clean with fewer particle additions while avoiding PICR, changes to critical dimensions, and changes to the dielectric constant.

NON-DAMAGING TO LOW-K FILMS

Several tests have been carried out to determine what effect, if any, CryoKinetic processing has on low-k films. We studied several low-k films, including fluorine-doped silica glass (FSG), as well as very low-k films, such as organic-doped silica glass (OSG), and ultra low-k films, such as porous hydrogen silsesquioxane (HSQ) and porous methyl silsesquioxane (MSQ). Measurements included FTIR and ellipsometry on blanket films before and after CryoKinetic processing. For comparison, these measurements were also made on films subjected to liquid cleaning processes.

FTIR measurements before and after CryoKinetic cleaning for undoped silica glass (USG) along with FSG and OSG are shown in Figures 6. FTIR measurements before and after CryoKinetic cleaning for porous MSQ and porous HSQ are shown in Figure 7. The FTIR spectra are virtually identical in all cases indicating that CryoKinetic cleaning has no impact on the chemical structure of the films. In contrast, Figure 8 shows the effect on FTIR spectra of liquid chemical cleaning for porous MSQ. In Figure 8, the FTIR difference spectra are shown. These spectra are obtained by first normalizing each spectrum according to the range of the absorbance value over the entire spectrum. Then a difference spectrum is calculated by subtracting the normalized value at each wavelength

of the spectrum taken before cleaning treatment from that taken after the cleaning treatment. It is evident from Figure 8 that CryoKinetic cleaning has little or no effect on the FTIR spectrum, whereas the various chemical cleans are affecting the Si-O bonding and Si-H bonding.

Blanket films were also characterized by ellipsometry. Table I shows the ellipsometric results before and after CryoKinetic processing. Again, no changes in the film are detected. Table II shows the ellipsometric results before and after ashing and liquid chemical cleaning. It is evident that ashing and wet chemical cleaning can have a significant impact on low k film properties whereas CryoKinetic cleaning has no effect.

SUMMARY

CryoKinetic cleaning has been successfully implemented as part of the Cu/low-k dual damascene BEOL. It has been proven to remove defects and improve final test yields in production when implemented as a pre-ILD clean. CryoKinetic cleaning is an effective technique for reducing defects and increasing product yields at many points in the IC manufacturing process without risk of damage or chemical attack.

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Table I. Ellipsometry measurements on films treated with the CryoKinetic process.

	film thickness (angstroms)		refractive index	
	pre	post	pre	post
USG	2640.15	2640.06		1.465
FSG	4618.47	4619.36		1.434
OSG	4337.38	4337.39		1.392
porous MSQ	4127.0	4125.6	1.258	1.258
porous HSQ	4106.3	4105.4	1.227	1.227

Table II. Ellipsometry measurements on films treated with reducing ash and chemicals

	film thickness (angstroms)		refractive index	
	pre	post	pre	post
porous MSQ + reducing ash	5710	5314	1.2625	1.2808
porous MSQ + reducing ash + chemical C	5710	4746	1.2625	1.2447

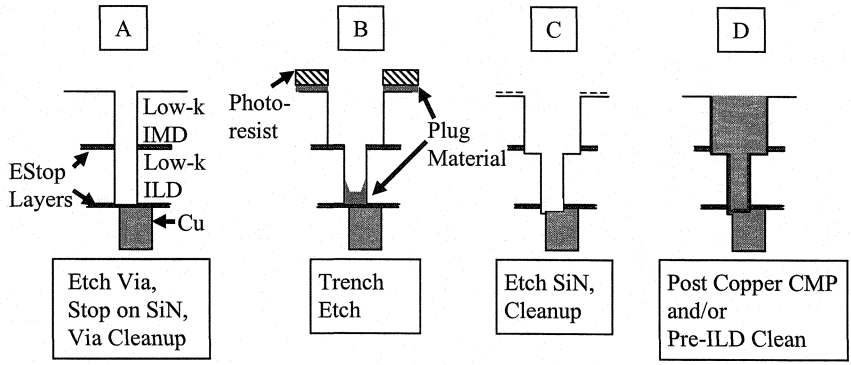
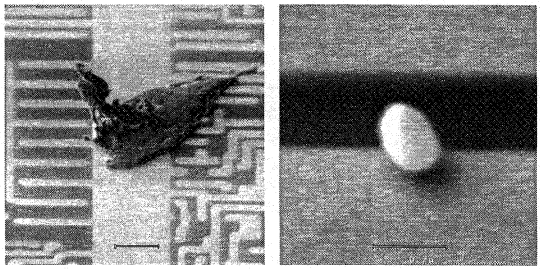


Figure 1. Clean opportunities with a Via-First, Cu/Low-k dual damascene integration scheme



(a) (b)

Figure 2. Typical defects that are removed by Ar/N_2 cryogenic aerosol cleaning. The defect on the left is approximately 10 microns wide while the defect on the right is approximately 0.2 microns wide

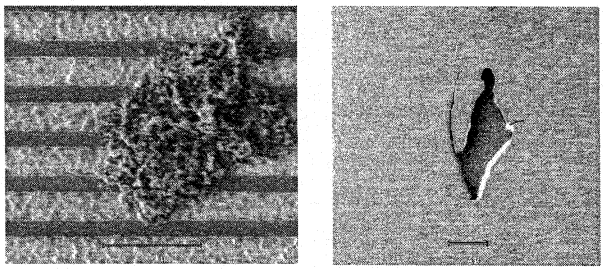


Figure 3. Non-cleanable defects include dried slurry residues and scratches or "ripouts".

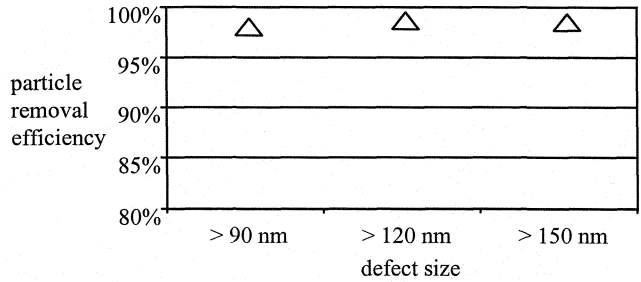


Figure 4. Particle removal efficiency measured on 300mm challenge wafers purposely contaminated with silicon nitride particles. Average nitride particle starting counts on fours wafers = 5177@>90nm, 4659@>120nm, 4149@>150nm.

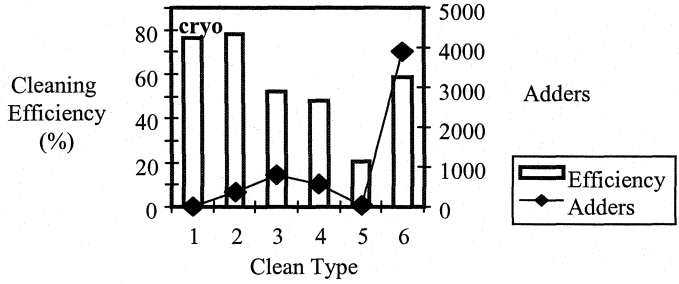


Figure 5. Cleaning efficiency for various pre-ILD cleans. Clean 1 is the CryoKinetic cleaning process. The other cleans are various standard wet cleans and brush cleans.

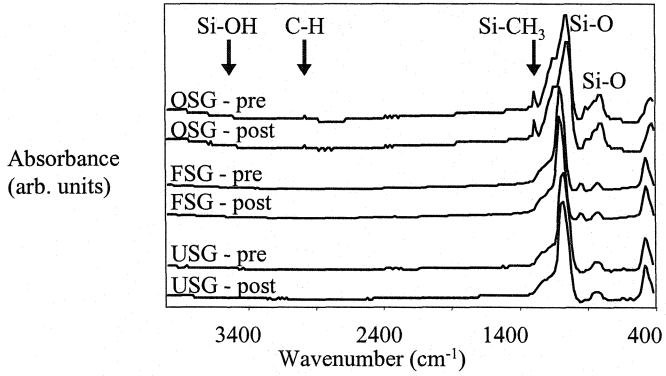


Figure 6. FTIR Spectra for films subjected to CryoKinetic Cleaning

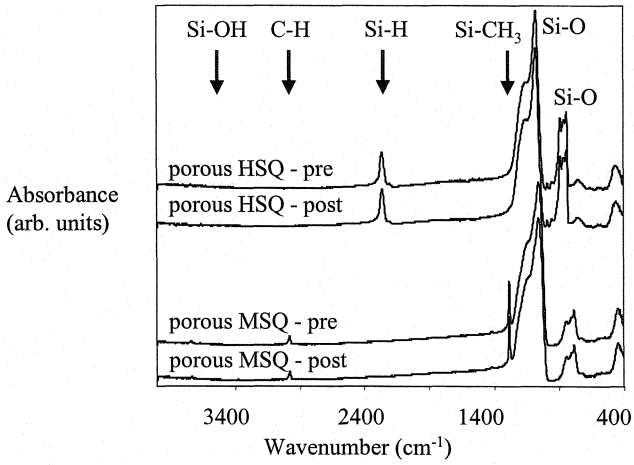


Figure 7. FTIR Spectra for porous MSQ and HSQ subjected to CryoKinetic cleaning.

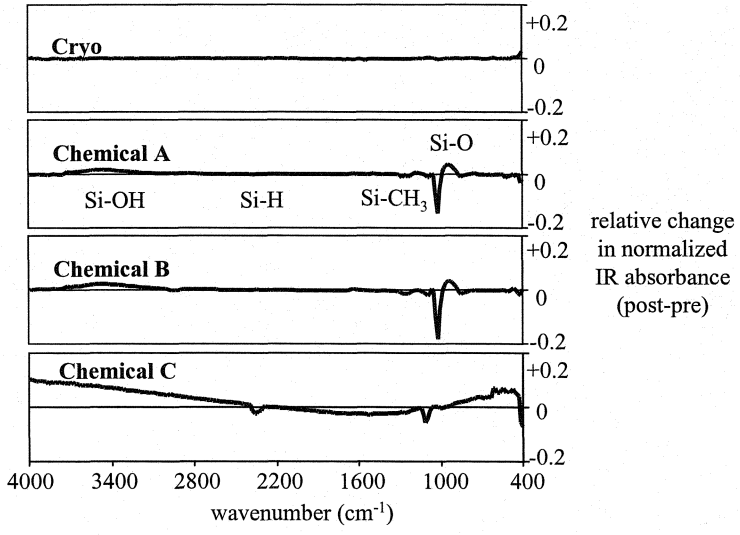


Figure 8. FTIR difference spectra for porous MSQ. Each FTIR spectrum is normalized and then the post spectrum is subtracted from the pre spectrum. CryoKinetic cleaning effects on the FTRI spectrum is compared to that of three liquid chemicals.

BACK-END CLEANS

SURFACE PREPARATION CHALLENGES WITH CU/LOW-K DAMASCENE STRUCTURES

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Competition is continuously driving die size smaller while at the same time customer demand drives higher levels of performance. In the recent past, these competitive forces resulted in metal pitch shrinking below 0.40um. At this pitch, subtractive aluminum metallization schemes ran into fundamental problems with Electro Migration (EM) performance which significantly impacted interconnect delay time. To meet these challenges, semiconductor companies are switching to copper dual damascene with low-k dielectrics. This paper will lead you through an explanation of what the industry has been doing for interconnect, listing some of the standard problems that occur, the fundamentals of Cu/low-k dual damascene and how this method modifies those same surface preparation challenges. In addition, a few of the new challenges this interconnect scheme creates will be identified. Documentation will be provided for specific challenges, the defects each challenge creates and the equipment and process design considerations required to avoid these defects.

INTRODUCTION

When cleaning wafers that use Cu dual damascene interconnects with low-k dielectrics, a whole host of problems can be encountered. These include the standard Back End of Line (BEOL) cleaning problems of low cleaning efficiency and excessive etch rates leading to shifts in critical dimensions. In addition, one must deal with preventing fab contamination, interface adhesion of new materials, dielectric stability, barrier integrity, Photo diode Induced Copper Redeposition (PICR) (1,2), and fundamental mechanical strength of 7+ layers of interconnect. Surface preparation interacts in new ways with each one of these issues creating significant challenges. The industry has a long way to go to make up for the 25+ years of maturity that was enjoyed with Al-SiO_2 interconnect.

WHAT HAS THE INDUSTRY BEEN USING FOR INTERCONNECT?

In order to understand where the industry is going, it is important to fully understand where the industry has been. Subtractive Al-SiO_2 interconnect integration schemes have

been used across the industry for over 25 years. To form a metal stack, in its simplest form, all manufacturers did the following: Deposit a metal film, pattern a metal film, etch the metal film, post etch clean (dry + wet), deposit an insulator, planarize the surface, and then start over. The metal film was typically Al-0.5%Cu sandwiched between TiN, Ti/TiN, or Ti, with either organic or lately, inorganic BARC (Bottom Anti-Reflective Coating) on top. These stacks were optimized for sidewall profile, sheet resistance, corrosion susceptibility, film adhesion, stress, EM performance and overall dielectric stability.

Contacts and vias were formed using a tungsten (W) plug process. W-plugs were created by etching a dielectric hole, performing a post etch clean, placing a barrier material down into this hole using physical vapor deposition (PVD), filling the hole with W by chemical vapor deposition (CVD), and then polishing the top surface off using Chemical Mechanical Polish (CMP). The CMP step serves to both separate the filled holes as well as planarize the surface. Even with Cu damascene integration schemes, W-plugged contacts are still in use. Figure 1 shows both the typical metal stacks as well as the cross-sections of W-plugged contacts.

Post etch cleans for both the metal stack and the via were combinations of ash, followed by solvents and/or dilute acids, many times followed by another ash. In some specific cases, the wet portion was a low temperature, concentrated acid mixture. Ash was dominated by oxidizing chemistries. Besides oxygen, additional gases such as nitrogen (as a dilutent), forming gas ($3\%H_2/N_2$), and most recently fluorocarbons were sometimes used. In most cases, the wet portion of the surface cleaning was performed utilizing an etch mechanism. In other words, etch the top surface of the film in question off (Al-0.5%Cu or dielectric), taking with this film the defects. For subtractive Aluminum metallization, this ended up driving slightly higher line resistance but fewer shorts and generally higher yield. From the via perspective, via size increased while resistance decreased. Negative impact on yield from via to unrelated metal shorting was not typically seen given the metal design rules used. In fact, contact and via cleans utilizing etch cleaning mechanisms usually resulted in higher yields.

WHY CHANGE TO CU/LOW-K DUAL DAMASCENE?

Given the 25+ years of experience with Al-SiO_2 integration schemes, why change? The answer is simple: To achieve higher device performance with shrinking geometries. Three major factors drive this performance increase. These factors are line resistance, intra-line capacitance, and EM performance. The combination of metal line resistance from Al-0.5%Cu, and intra-line capacitance from standard k dielectrics, has become a significant factor in circuit delay. Sheet resistance of Cu is approximately 33% lower than sheet resistance of Al. Dielectric permittivity directly feeds into capacitance. Since time for a circuit to propagate through an interconnect route is proportional to Resistance

multiplied by Capacitance (R*C), decreasing both R and C creates a faster device. Figure 2 shows a plot of circuit delay time versus metal pitch.

Cu dual damascene also benefits from changing from W-plugged vias to vias filled with Cu. In this case, the change in resistance is even more dramatic. Figure 3 shows a comparison of via resistance between Cu and W-plugged vias. Note, even though the Cu via resistance is >5X lower than W, the comparison is not even. The Cu via is both smaller and has a higher aspect ratio than what was measured for the W via. Both factors tending to enhance the apparent performance of the W-plugged via shown in Figure 3. This same performance improvement can be seen when comparing Cu to Al-0.5%Cu vias for EM performance. Figure 4 shows approximately a 10X improvement (for the entire distribution) in EM performance for Cu vias relative to Al-0.5%Cu. The best vias show nearly an 80x improvement.

When Cu dual damascene was originally proposed, there was yet another reason stated as to why the industry should change. Lower Cost of Ownership (CoO). While it was hoped that Cu dual damascene would result in lower CoO, from a supposedly simpler process flow, this has not been the case. As it turns out, the increased complexity in several areas including surface preparation have resulted in some increase in CoO along with the increased performance.

POTENTIAL DUAL DAMASCENE INTEGRATION METHODS

Copper dual damascene can be implemented many ways. The four most common integration schemes are labeled self-aligned, partial (or half) via first, via (or full) first, and trench first. Of these, the most common are partial or full via first. All of these schemes utilize a stack with a via etch stop that doubles as a Cu diffusion barrier and some sort of ILD/IMD stack. Within this ILD/IMD stack there may or may not be a trench etch stop and a top hardmask layer. Each of these potential changes to the integration scheme have implications on what constitutes the best cleans process. In all cases, there are at least four cleans (Figure 5) and as many as six cleans required to complete one interconnect level with associated Vias. Cleaning needs include post CMP (Cu and possibly ILD polish), pre-ILD, pre-IMD, post via, post trench, post etch stop, and pre-PVD. Each of these cleaning needs may be a single or a multi-step clean sequence.

KEY CU/LOW-K CHALLENGES WITH ASSOCIATED DEFECTS

Cu/Low-k dual damascene requires fundamental change to past cleaning strategies. Besides the standard cleaning issue with minimizing defectivity, there are many new

challenges and old challenges requiring very different solutions. Rather than attempt to prioritize which challenge is most important, challenges with associated defects will be addressed in no specific order.

Copper does not self-passivate as Al-0.5%Cu does. Where Al builds up a passivating oxide, copper continues to oxidize whenever exposed to an oxidizing ambient. Unfortunately, copper oxide is not a good conductor. This requires a specific strategy to deal with oxidized Cu. Multiple solutions exist. Some of these solutions include minimizing the number of times Cu is exposed to cleans, using reducing chemistries instead of oxidizing chemistries, using reducing chemistries after oxidizing chemistries, removing oxidized Cu using wet chemistries that are selective to Cu while maintaining high etch rates on copper oxide, or physically removing oxidized Cu with a pre-sputter etch (pre-PVD) clean. The best solution is largely dependant on the integration scheme used.

In addition to the oxidation type of corrosion phenomena, Cu is susceptible to PICR (1, 2). Whenever Cu lines are in close proximity, are connected to a large silicon photo-diode, and have any light present (Si bandgap is 1eV, all visible light exceeds 1eV energy level) the possibility for PICR exists. Figure 6 illustrates how Cu(2+) can drift and/or diffuse away from a Cu anode redepositing on a cathode. Since the electric-field lines in the dielectric are primarily perpendicular to the Cu(2+), the drift component is negligible. Where the same is largely true for the diffusion component in a dry environment, diffusion can be significant in a wet environment. Figure 7 shows top down SEM pictures with Cu-leads connected across a large photo-diode. Several solutions can be implemented to meet this challenge. By far the simplest is to perform all wet processing in the dark thus insuring no light reaches the photo-diode. Of course, this can have significant tool implications. This approach can be modified to use standard tools that are not dark whenever Cu is not exposed. However by doing so, there is risk of accidental exposure with associated damage due to any process excursions.

Preventing Fab cross-contamination has been an on-going challenge for years. Everyone has heard of Fabs that have been completely shut down by contamination incidents resulting in thousands of scrapped wafers, numerous tool wet cleans, replacing most if not all of the Fab's quartzware, many-many hours of downtime and millions of dollars in lost revenues. In the past, these incidents were mostly related to accidental contamination from unknown metals or sodium (Na) contamination. Now, Cu is being deliberately introduced into the process flow. Since Cu has a higher diffusion constant than Na, this can be a challenge. Solutions must take into account both prevention and mitigation. Prevention takes the form of strict limitations for equipment usage between Cu portions of the flow and non-Cu portions (including Al). The criteria to not process both Cu and Al based interconnects in the same processing tools assumes barriers capable of preventing Cu diffusion are not implemented on Al based process flows. Rigorous cross-contamination testing should be performed on any tools that are shared. Mitigation most often takes the form of cleans targeted exclusively at the wafer backside. Backside

copper removal cleans enable additional tool sharing. This significantly eases restrictions on many low temperature tools such as metrology and photolithography.

Interface adhesion of new materials has also been an on-going challenge for years. The difference with Cu/low-k dual damascene is the number of new materials, the generally reduced adhesion of almost all low-k materials and the increased number of interfaces involved. Other process areas tend to be primarily responsible for basic material properties. Surface Preparation can impact the situation by controlling the frequency, duration, and chemical selectivity of those cleans exposed to the interfaces in question. Figure 8 shows top down SEM and cross-section TEM photos of a SiN barrier delaminating off the top of a large Cu area. By controlling the chemistry, duration, and frequency of cleaning chemistry exposure, delamination was eliminated.

The significance of fully drying the wafers has never been so acute. Ultra-Low-k (ULK) dielectrics tend to be porous by nature. Though suppliers of some of these materials claim to have materials with closed pores, most acknowledge some percentage of open pores. To further exacerbate the situation, many of these ULK materials have organic functional groups such as methyl added to reduce k. Methyl groups cause the surface to be hydrophobic. Combine open pores with a hydrophobic surface and most forms of conventional drying become obsolete. Figure 9 shows a FTIR spectra of wafers treated with a reducing ash, then various wet chemistries followed by commercially available dryer. As can be seen, the Si–OH peak around 3400 wavenumbers is still noticeable. The addition of water to these films increases the k values.

Barrier integrity is critical to prevent Cu migration to transistors. Any process (such as etch, ash, pre-sputter etch, ...) using a strong physical component may tend to sputter Cu onto feature sidewalls. If this occurs before the barrier layer is deposited, this Cu is effectively under or outside the barrier at time zero. The surface preparation challenge is to remove Cu containing residues from the feature sidewalls while preserving any exposed Cu at the bottom.

Critical Dimension (CD) control is another one of those on-going challenges. The first few layers of interconnect (signal leads) typically are designed at minimum photo capability. In the past, most wet portions of the surface cleaning was performed utilizing an etch mechanism. In other words, etch the top surface of the film in question off (Al-0.5%Cu or dielectric), taking with this film the defects. For subtractive aluminum metallization, this ended up driving slightly higher line resistance but fewer shorts and generally higher yield. This phenomena works exactly the opposite for dual damascene. Now, etch mechanisms increase metal and via CDs. This increases capacitance and decreases yield from increased via chain and comb-serpent shorting. This tends to focus cleans on mechanisms that utilize solvation or swings in surface charge to clean the surfaces.

Dielectric damage from dry cleans is one of the new challenges with Cu/low-k dual damascene. Many materials utilize doping additions of F or C and/or the addition of methyl groups (-CH3) to decrease k values. Unfortunately, many etch and ash processes tend to remove these additions from the materials while degrading electrical properties. The result is enhanced wet etch rate, increased k and increased leakage. This same plasma damage further exacerbates film etch rates impacting CD control. Table 1 shows the impact from dry and wet clean steps on VLK wet etch rates. The major impact on wet etch rates comes from previous dry plasma processing. The proposed goal for shift in k per level in the 2001 ITRS is 5.0% from all processing. This same proposal suggests cleans can account for no more than 50% of this or a 2.5% change.

Finally, the last challenge for Cu/Low-k dual damascene is increased susceptibility to surface defects. In the past, once a particle landed on the surface of a wafer it could be immediately classified as either a "killer" or a "benign" defect. For dual damascene, this is not the case. If at time zero, surface particles do not create shorts or opens, these particles can still be encapsulated by the dielectric. The encapsulated particle can then interact with the CMP steps possibly leading to rip-out defects. Figure 10 tracks both a particle and a micro-scratch through the process flow illustrating how these become shorts or "killer" defects.

TYPICAL DEFECTS

Cu/Low-k dual damascene can have many different kinds of defects. Ten of the most common types are shown in Figure 11. Some of these defects are shown as they would appear in-line at the point of occurrence (Figure 11 e, h-j). Others defects are shown as detected after end of line Physical Failure Analysis (Figure 11 a-d, f). Common defects include electrochemical deposition voids, missing via patterns, ILD/metal rip-outs, floating or incomplete vias, missing trench patterns, missing contacts, incomplete Cu CMP, surface particles, surface flakes, and polymer strands. Only one of these defects does not have a potential tie-in to surface preparation. That is incomplete Cu CMP. All the other defects, have potential surface preparation mechanisms.

For ECD voids, one mechanism is to have incomplete polymer strips. These residual polymers then block or shadow the PVD barrier/seed deposition. Without a seed, the Cu will not plate into that feature. Missing contact, via, or trench patterns can have many causes. Surface preparation itself may impact missing patterns multiple ways. Everything from leaving surface particles or flakes, leaving chemical residues that later poison DUV photoresist, or by the use of nitrogen in the dry-clean plasma that can lead to later amine out-gassing and poisoning of DUV photoresist and even our old nemesis watermarks (circular drying residues on hydrophobic surfaces). ILD/metal ripouts has already been discussed above. Floating or incomplete vias is another one of the common defects that can have many causes. From a surface preparation perspective, floating vias

is most likely due to some sort of blockage. Besides the particle, flake and poisoning mechanism discussed already, simple incomplete residue removal from a previous post etch clean can create this defect.

SUMMARY

Copper , low-k damascene integration is starting to be implemented industry wide. It has shown to be an effective integration scheme that enables increased device performance but at a higher CoO due to process complexity. Some of this increased complexity negatively impacts surface preparation. Negative impact takes the form of decreased compatibility with cleans based upon etch mechanisms, increased yield sensitivity to both surface and embedded defects, and less multi-node cleaning solutions due to different surface chemistry accompanying different low-k materials.

In response surface preparation strategies are shifting. For ashing, temperatures and pressure are being reduced, chemistry is shifting from oxidizing to reducing, and possibly for the first time etch selectivity has become a fundamental performance metric at ash. For wet cleans, process control requires the control of ambient gas mixtures and light conditions along with some form of enhanced drying. Chemistries are increasingly using exotic buffering agents to enable fluoride introduction. These changes create opportunity for fundamental shifts in tool strategies. Batch moving toward single wafer. Immersion going to spray (or vice versa). Introduction of novel clean methods that fundamentally address these challenges such as cryogenic aerosol or electro hydro dynamics. Or is this the time for the leap to combined dry and wet cleaning? Only time will tell. No matter what else happens, with the introduction of ultra low-k materials, wafer drying will never be the same again.

ACKNOWLEDGEMENTS

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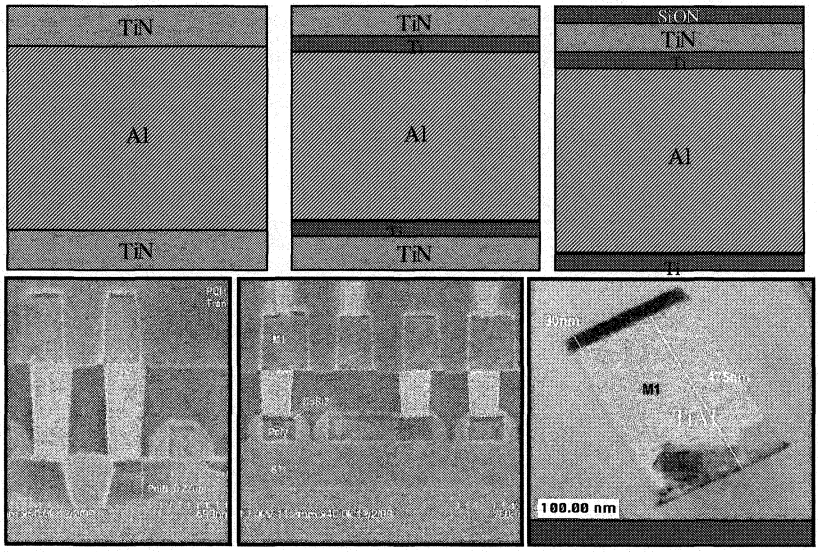


Figure 1. Typical Al/0.5% Cu metal stacks along with cross-sections.

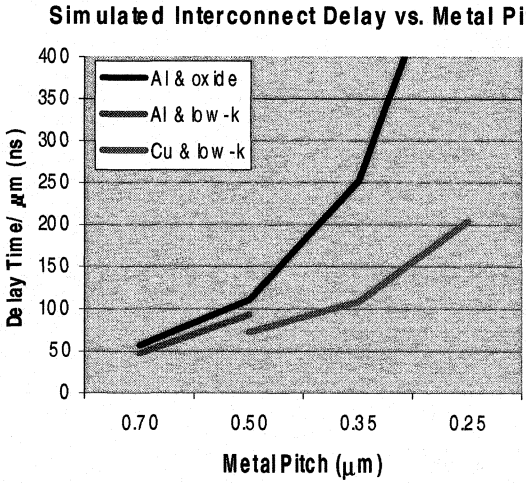


Figure 2. Simulated interconnect delay time versus metal pitch.

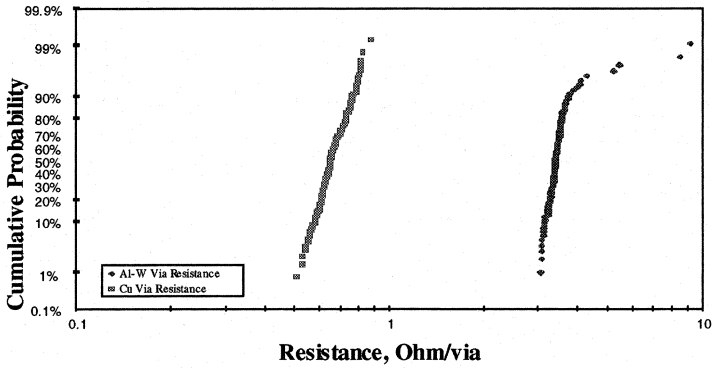


Figure 3. Comparison of via resistance with Cu (0.24 um, 4.7:1 AR) and with Al-W (0.26 um, <4:1 AR). Cu vias show 5X lower resistance than W vias.

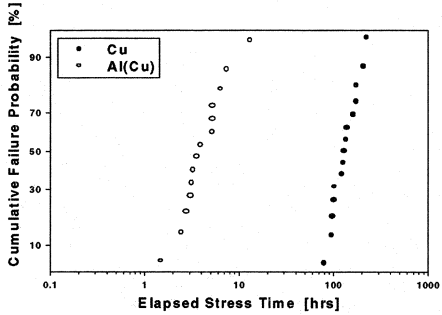


Figure 4. Cu versus Al-0.5%Cu Electro-Migration performance. Cu shows significant improvement in EM performance even with an immature process.

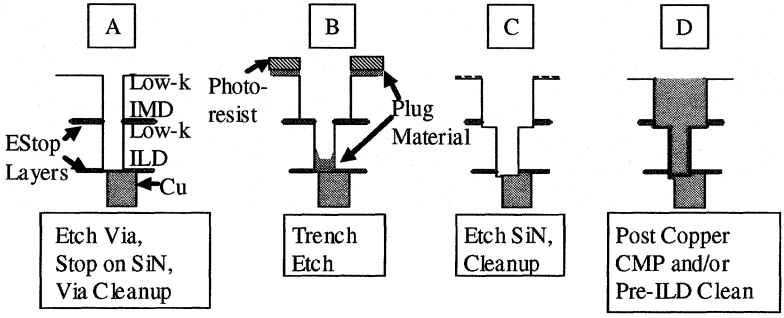


Figure 5. Cleaning needs with a Via-First, Cu/Low-k dual damascene integration scheme

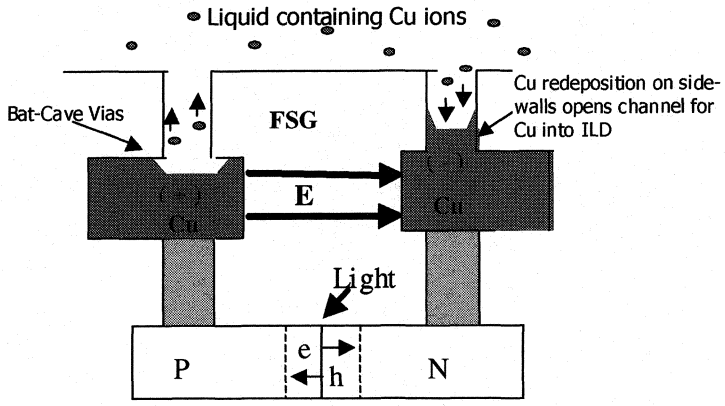


Figure 6. Photodiode-Induced Cu Redeposition (PICR) inside a via.

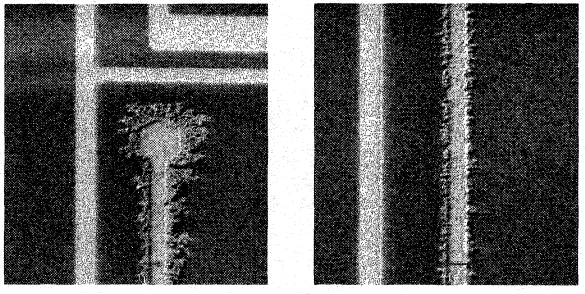


Figure 7. PICR example. Cu trenches contacting N-well, photo diode turned on.

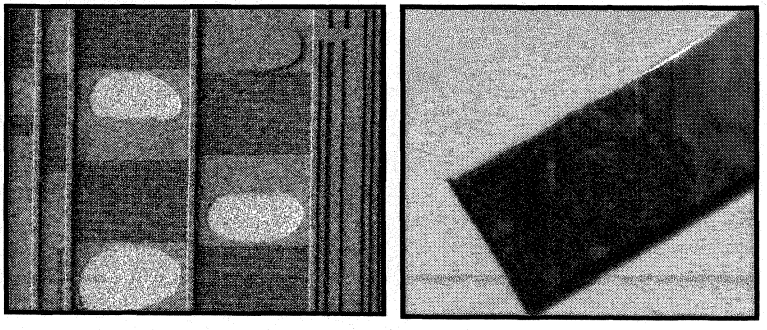


Figure 8. Top down SEM and cross-section TEM showing interface adhesion problems on a Cu/Low-k device. Barrier delaminating off the top of Cu.

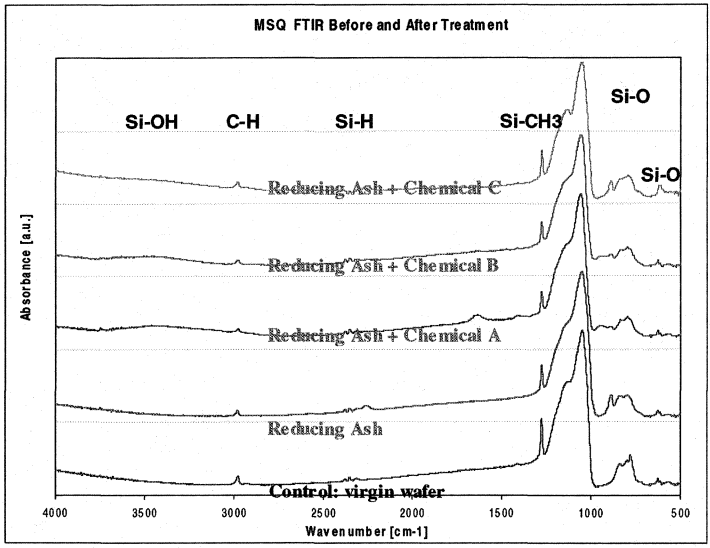


Figure 9. Porous MSQ film change versus cleans by FTIR. Significant film change apparent versus clean treatment.

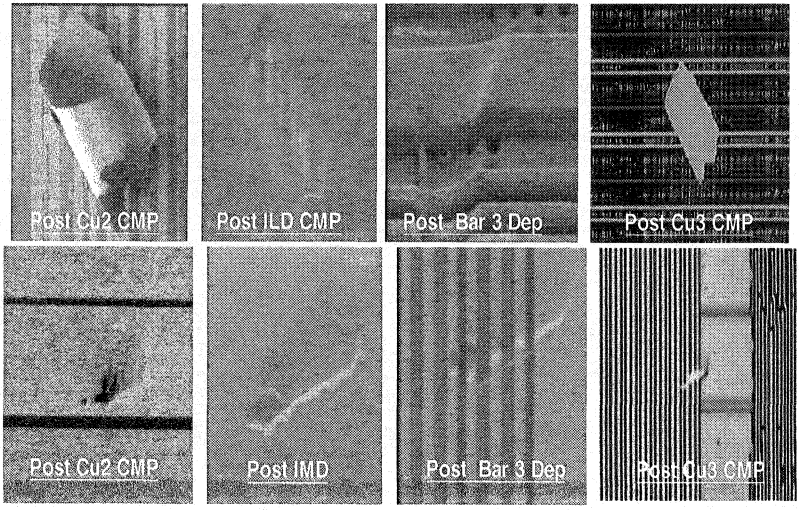
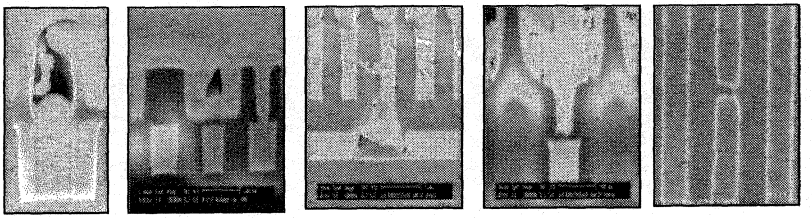
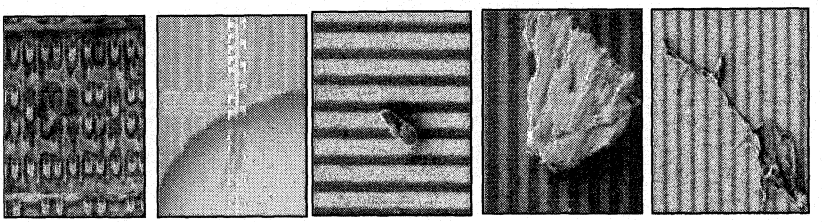


Figure 10. Partitioning test from M2 to M3 CMP showing how particles top) and scratches (bottom) can cause shorts.



a. ECD voids | b. Missing Via Pattern | c. ILD/Metal Rip-out | d. Floating Vias | e. Missing Trench Pattern



f. Missing Contacts | g. Incomplete Cu CMP | h. Surface Particle | i. Surface Flake | j. Polymer Strand

Figure 11. Ten of the most common Cu/low-k dual damascene defect types.

Process	Pre-Thickness	Post-Thickness	Delta Thickness
3' Solvent Strip	5056	5054	-2
3' Reducing Ash	5054	4830	-224
Reducing Ash + Solvent	5057	4803	-254

Table 1. Impact from plasma steps on VLK wet etch rate. Data shows majority of impact from plasma step. Dry step film modification increased wet etch rate by ~15X.

POST ETCH/ASH CLEANING OF DUAL DAMASCENE STRUCTURES: SINGLE WAFER MEGASONICS WITH STG DRY

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Megasonics and surface tension gradient (STG) dry technology have been integrated into a single wafer cleaner. Post etch/ash cleaning of dual damascene structures has been enhanced by both technologies. In addition to the advantages of a single wafer cleaner, the megasonics and STG dry improves cleaning efficiency by: (1) increased chemical transport rates to and away from the surfaces inside the via, resulting in significantly decreased process times, (2) improved particle and residue removal and (3) drying without rinse residue in the via. SEM and electrical results are shown to illustrate the impact of the integrated technologies.

INTRODUCTION

In Cu processing, a wet clean is commonly used after etching and ashing of the dual damascene structure. Removal of etch and ash residue as well as copper contamination sputtered on the sidewalls is required. Without the clean, a significant yield impact is observed. A number of semiaqueous solvents have been designed for these purposes. The chemicals are used in both batch (spray and immersion) and single wafer cleaning tools. For sub 0.18um technologies, there is an increased use of single wafer tools due to improved process control, reduced cross contamination and reduced process cycle time.

Megasonics are widely used in batch cleaning to improve particle removal performance [1] A new single wafer megasonics was developed to expand this technology to single wafer cleaners. Advanced dual damascene cleaning has an additional challenge: the megasonic energy must be controlled in order to avoid damage of the sensitive dielectric between the trenches.

Surface tension gradient dry is also widely used in batch immersion cleaning [2]. Introduced here is a single wafer drying method [3] which relies on the rotational and Marangoni forces to dry the wafer without evaporation. Eliminating evaporation allows drying without leaving residue that was dissolved in solution.

EXPERIMENTAL

The megasonic assembly (figure 1a) consists of a piezoelectric transducer attached to the end plate of a quartz rod. The rod is placed slightly above a horizontally positioned wafer. Sound transfer occurs through a liquid meniscus between the wafer and rod. Liquid is also sprayed on the backside to allow the energy to pass through the wafer and remove particles on the backside. The wafer is dried using a surface tension gradient method (figure1b). A mixture of nitrogen, isopropyl alcohol is directed to the wafer center through a nozzle. Water is dispensed through a second nozzle just outside the N_2/IPA nozzle. As the wafer rotates, the nozzles are moved towards the wafer edge to complete the dry.

Dual damascene patterned wafers with different dielectrics (k = 4 to sub 2.6), via dimensions (0.4um to sub 0.15um openings), and aspect ratios were cleaned on the single wafer megasonic cleaner (Goldfinger). A typical process is: step 1 – megasonic clean with commercially available semi-aqueous solvent (chemical A or chemical B) dispensed on the wafer at low rotation speed (20 rpm); step 2 – high speed spin to remove majority of chemicals; step 3 – rinse at high speed, followed by lower speed meg rinse; step 4 - STG dry. Wafers results were evaluated with SEM and via contact resistance. SEM (top-down, angled and cross-section views) were taken before and after cleaning.

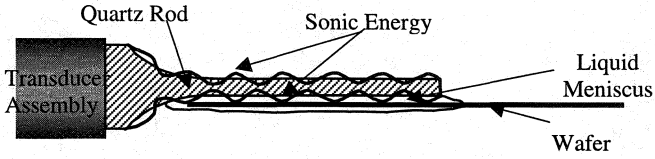


Figure 1a. Megasonic schematic

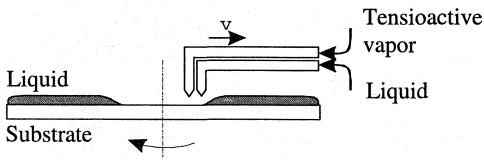
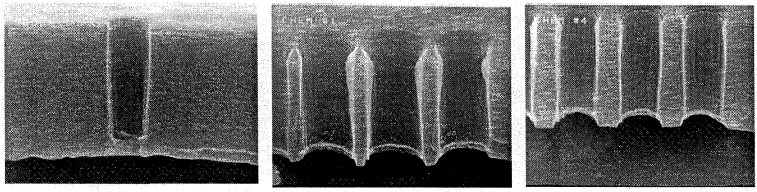


Figure 1b. STG dry schematic

RESULTS AND DISCUSSIONS

Via and trench cleaning examples

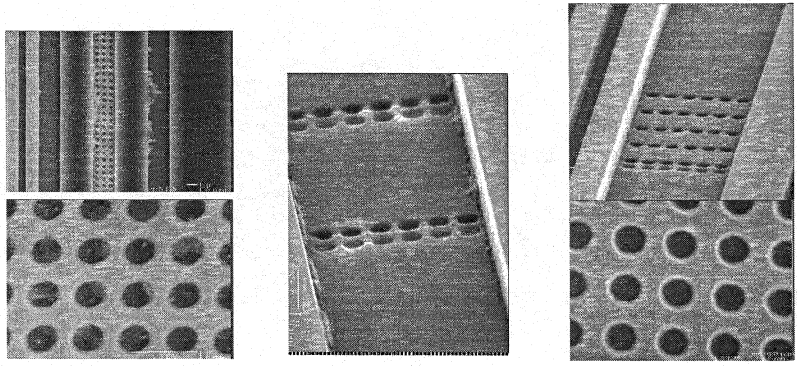
Figure 2 shows the impact of megasonics on the removal of contamination from the via bottom. Experiments had identical conditions (rinse and dry recipe and chemical type and temperature), with the exception of megasonics (on or off) and chemical process time. Cleaning of the 0.15 μm vias was accomplished more effectively and in a shorter time than the non-megasonics case.



Pre-clean | **60 sec. Chemical A without megasonics** | **37 sec. Chemical A with megasonics**

Figure 2. Cross-section via SEMs of pre-clean and post-clean samples. The SEM pictures were taken at tilted angles.

Figure 3 shows the impact of megasonics on contamination at the top of the via, around the edge. Top-down view SEMs of (a) un-cleaned, (b) 5 min immersion clean in chemical B, (c) 90s megasonic clean in chemical B.

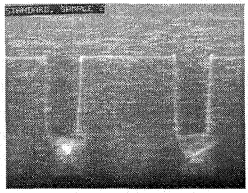


(a) Un-cleaned | **(b) 5 min. immersion in chemical B, 1 min. IPA rinse and 3 min. DI rinse** | **(c) 90 sec. Chemical B with megasonic, 30 sec. DI rinse**

Figure 3. Top-down view SEMs of un-cleaned and cleaned samples.

Figure 4 demonstrates the ability of the single wafer cleaner to remove contamination remaining after silicon nitride breakthrough. The contamination at the bottom of the sub 0.18μm vias was removed following a 90s megasonic clean process. The process time was not optimized, but is expected to be in the 30s range.

Pre-clean



Post-clean (90sec. Chemical A with megasonics, 30sec. DI rinse)

Figure 4. pre and post clean cross-section SEMs of vias in dual damascene structures.

Mass transport

Megasonics improves both mass transport of the chemicals to the surface and removal of the chemicals and rinse agent away from the surface. The impact of megasonics on the boundary layer is shown in table 1 [4]. It has also been physically modeled that rinse flow with megasonic pulsation can greatly improve rinse efficiency on sub-micron size trenches compared to steady rinse flow [5]. More efficient transport of chemicals to the surface and contamination away from the surface can significantly reduce process times leading to higher throughput and therefore lower cost of ownership.

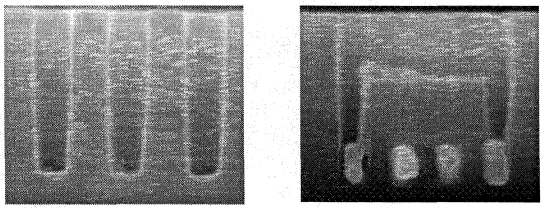
Condition	Boundary Layer thickness
Typical recirculation bath	3000 μm
Very strong stirring	300 μm
Megasonics @ 850 kHz	0.6 μm

Table 1. boundary layer with and without megasonics

Surface tension gradient dry

Drying by surface tension gradient (STG) rather than by spin or evaporative methods has been shown to give improved results in batch systems. STG dry offers the complete removal of the solution. Spin drying removes much of the liquid by evaporation, which causes some dissolved materials to remain on the wafer and form watermarks. The resulting watermark from spin drying can cause masking problems in subsequent steps,

and the chemical residue can increase the via contact resistance. It is especially true for narrow, high aspect ratio vias which are more prone to trap chemical residues inside during spin dry, if the rinse does not completely eliminate chemical residues from vias. As the aspect ratio of the via increases, the performance difference between the STG dry and the spin dry increases. Table 2 summarizes the 0.19μm and 0.38μm via contact resistance results. The same process was used for all, with the exception of the dry method. Although the recipe was not optimized, it allows for demonstration of the difference in dry methods. The electrical results have shown that when the STG dry was used, better performance is obtained for both via sizes in terms of reduced contact resistance and improved process uniformity. SEM results seem to support the electrical results. Figure 5 shows the cross sectional SEMs of 0.19μm vias that were spin dried and STG dried after a 60 sec chemical process and a 20 sec DI rinse. Visible contamination was observed at the via bottom in the spin dry case.



(a) Spin dried (b) STG dried

Figure 5. Cross sectional SEMs of 0.19 μm vias that were dried with (a) spin-dry and (b) STG dry after a 60 sec. Chemical process and a total 20 sec DI rinse.

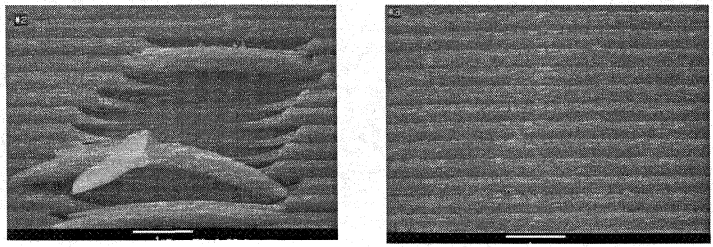
		0.19 μm		0.38 μm	
		Mean	**IQR**	**Mean**	**IQR**
2 min chemical A + 20sec DI rinse	**Spin** dried	1.53	0.68	1.20	0.27
	STG dried	1.00	0.26	1.00	0.18

Table 2. single via resistance measurement results (normalized) of differently dried wafers

Damage-control tests

Although megasonics improves particle removal and mass transport, it can also cause damage to sensitive structures, including the low-k dielectric material between trenches. Single wafer megasonics allows for significantly more sound uniformity control than a batch methods[6]. However, even single wafer megasonic system used incorrectly can cause structural damage. Proprietary methods and configurations have allowed for the

cleaning advantages without damage. Shown in figure 6 is an experiment on sensitive low-k serpentine line structures. Two different conditions were used. An example of the potential damage is shown in figure 6a. The undamaged dielectric obtained when using the controlled megasonic process condition B is shown in figure 6b. Development work is being performed to provide damage-free cleaning for advanced porous low k materials.



(a) Condition A (b) Condition B

Figure 6. Top-down view SEMs of samples tested under (a) non-controlled condition A, and (b) controlled condition B.

CONCLUSIONS

Cu dual damascene cleaning has been enhanced by single wafer cleaning with integrated megasonic and STG dry technology. The technology is most critical for advanced devices with small vias. Shorter process times and improved cleaning is provided by the megasonic technology. Controlled megasonics conditions and configurations are required to provide the cleaning benefits without structural damage to the wafer. STG drying provides a significant improvement in residue-free drying as compared with spin drying.

ACKNOWLEDGEMENT

The authors would like to thank our colleagues Mike Olesen, Tom Nicolosi, and Rich Wiley for valuable advice and support on this work.

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IMPROVED POST-ETCH VIA CLEAN WITH FLUORIDE-BASED SEMI-AQUEOUS CHEMISTRY USING AN INTERMEDIATE RINSE

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An improved post-etch via cleaning process is studied using a fluoride-based semi-aqueous chemistry in a multi-position spray processing tool. The process uses two separate dispense steps of the semi-aqueous chemistry, with an intermediate deionized water rinse. Inclusion of the intermediate rinse significantly improves the removal of post etch residues. This improved cleaning is likely due to a diffusion process by which a layer of initial by-products is rinsed away by the intermediate rinse. The underlying contaminants are then exposed to the second chemical dispense step allowing complete removal. The combined time of the two separate chemical dispenses is much less than the time required for a single chemical dispense process.

INTRODUCTION

Over the past ten years hydroxylamine-based chemical systems have become industry standard in post etch residue removal. While standard amine-based and hydroxylamine-based chemistries have shown good cleaning performance, they require elevated temperatures (~60° C) and extended process times (15-45 minutes). Also, rinsing with alcohol or a buffered solution is required before water rinsing to avoid a pH spike which can lead to metal corrosion. These conditions and requirements are challenging for cleaning equipment design and control.

Recently, fluoride-based semi-aqueous cleaning (SAC) chemistries have been introduced for both post metal etch residue removal and post via etch residue removal. Fluoride based chemistries have been designed for both wet benches and spray tools. These chemistries can be used for low- or room-temperature processes with shorter process times, are able to be rinsed in water and can reduce water-rinse volumes. Most of the semi-aqueous fluoride chemistries can be used at near ambient temperatures (23 to

30° C) with process times varying between 2 to 30 minutes. Semi-aqueous fluoride chemistries are composed of organic solvents, water, low concentrations of fluoride species and buffering agents to control the fluoride chemical activity. These semi-aqueous chemistries have pH ranges between 9 to10. This class of chemistries is showing good cleaning ability not only on metal (Al, Ti, W and Cu) and via structures but also with many new low k materials and unlanded metal lines on W plugs (1).

Usually, the wet chemical cleaning process for post- etch residue (PER) removal is optimized as two separate steps – cleaning and rinsing. The first step involves removing the etch residue with an active chemistry (such as a hydroxylamine system or a fluoride-based system). The second step involves rinsing away the cleaning chemical and reaction byproducts. In the case of hydroxylamine systems, if the process tool cannot efficiently remove chemical from the wafer surface before water rinsing, a two step rinsing process of alcohol followed by water is required. Commonly, the cleaning and rinsing steps are separately optimized to first remove residues without attacking the desired structures and then to remove the chemistry without causing pH excursions.

This approach to process optimization has been successful for traditional amine-based and hydroxylamine-based chemistries since they operate by dissolving the post etch residues from the outer surface inward to the walls of the via structure. In contrast, semi-aqueous fluoride chemistries tend to clean IC metal structures by a diffusion process. As the chemistries diffuse into the PER, the "polymeric" inorganic/organic residues are converted into smaller subspecies. Because of the low water content in the chemistry only a small portion of these "subspecies" is dissolved. Most of this converted material remains in place until the DI water rinse step (2). As this layer builds up, the cleaning reaction slows down and can lead to extended process times in order to achieve complete residue removal.

It has been found that introducing an intermediate rinse, between two separate chemical dispense steps, is an effective means for efficiently removing cleaning byproducts and reducing overall chemical exposure time. The use of a spray acid processor for PER removal enables the simple introduction of this intermediate rinse.

EXPERIMENTAL

A chemical recirculation system is used to dispense the SAC from a temperature controlled reservoir (3). Figure 1 shows a schematic of the spray acid processor with an integrated recirculation system.

The initial test involved a one step chemical dispense ambient temperature (23° C). Chemical was dispensed for 5 minutes. A DI rinse and dry sequence followed. SEM inspection showed residue remaining on the bottom of the via. In the next test, an

intermediate DI water rinse was inserted between 2 chemical dispense steps of 2 minutes each. SEM analysis show that the residue had been removed from the via. Each test above was repeated twice with similar results. An hydroxyl-amine based chemistry was also evaluated in this experiment. It proved capable of cleaning the residue in the via with a chemical dispense time of 20 minutes at 75° C. A buffered (pH~4) intermediate rinse solution was used between the chemical dispense and the final rinse.

The optimized process involves two chemical dispense steps with an intermediate DI water rinse step between them. It ends with a final DI water rinse and dry. The first chemical dispense uses a 90 second dispense of the recirculated semi-aqueous chemistry, followed by a chemical reclaim step. The chemical reclaim step conserves the recirculated chemical and reduces the interaction between the chemical and the DI water. The intermediate rinse is a 30 second rinse with DI water and is followed by a high speed spin step to remove DI water. As with the chemical reclaim step, the DI water is spun off in order to minimize the interaction between the water and the chemical. The second chemical dispense is identical to the first chemical dispense. The process then finishes with a "ramped rinse" and dry sequence. The chemicals are dispensed at a high rate of flow (10 liters/minute) while the wafers are rotating at a high spin rate (500-rpm). The intermediate DI rinse is also dispensed on wafers at a high spin rate. The combination of high spin rate and high flow rate enables a rapid turnover of solution in the via holes.

RESULTS

SEM Analysis

Figure 2 shows the initial condition of a via wafer after etch and ash processing. The polymer is raised up from the bottom of the via. This is the result of the back sputtering and redeposition of material onto the eroding photoresist of the via mask during the plasma etch. The bulk of the photoresist is removed in the ashing process, leaving the polymer residue behind. At this stage the polymer is composed of inorganic aluminum and titanium metal oxides and silicon oxide along with a mixture of organic material not removed in the ash (4, 5).

The results of the improved process, shown in figure 3, can be contrasted with the results of a process in which the semi-aqueous chemical was dispensed continuously for 5 minutes and then rinsed and dried. (Figure 4.) The continuous dispense process chemical dispense time longer, yet it does not remove the post etch residue. The intermediate rinse process is faster and more efficient than the continuous dispense process. There is no obvious corrosion damage to the underlying metal in either process. Via dimensional gain, due to interlayer dielectric etch, is also minimal.

Intermediate DI Rinse Theory

As stated above, semi-aqueous fluoride chemistries clean IC metal structures by a diffusion process. As the chemistries diffuse into the PER, residues are chemically modified and the cleaning process slows as reaction byproducts accumulate. By removing the soluble residue, the intermediate DI rinse enables this process to continue more efficiently during the next chemical dispense.

During the intermediate rinse, DI water is dispensed on to the wafers from a center spray post at a high flow rate. The wafers are set in a turntable spinning at a high spin speed. The "carry over layer" – the liquid layer of process residue on the surface of the wafer - is around 2um thick. This is due to the centrifugal force generated by the high-speed rotation of the turntable. The thin carry over layer leads to rapid dilution of the residual SAC chemistry and dissolved PER on the wafer surface and in the via as the intermediate rinse is initiated. The carry over layer is continuously refreshed with clean DI water (6). Analysis has shown that deep trenches (4 um deep x 0.5 um wide) are easily rinsed to equilibrium in less than 1 second time (7). Also the SAC contain no significant amine species to form additional corrosive hydroxide species in rinse water. Adding water to these SAC formulations does not increase the pH above its initial value. The formulation of the semi-aqueous fluoride chemistry, along with quick chemical dilution, reduces the potential for corrosion of the aluminum/copper metal at the bottom of the via. The HDA chemistries, on the other hand, can experience pH shifts up to 10.7 to 11.5 which can be corrosive to Al metal and many low k materials

The final rinse sequence is also critical. It starts after the second semi-aqueous chemical dispense with a high spin speed and a high DI flow rate. This is followed by "ramped" rinsing sequence and then the wafer dry. Again, the rinsing sequence focuses on rapid solution turnover in the via along with the diluting and cleaning properties of the "ramped" rinse. The final rinse time is kept to a minimum in order to balance the exposure of the metal at the bottom of the via to the DI water with the necessary cleaning of chemicals from the process chamber.

SUMMARY

The use of an intermediate DI rinse in a post-etch via cleaning process using fluoride-based semi-aqueous chemistry has been demonstrated. The improved via clean process uses the intermediate rinse to take advantage of the diffusion activity of the cleaning chemistry. This process sequence has proven to be faster and more efficient than a single step dispense process. The improved post-etch via clean process with semi-aqueous chemistries is a viable option to the standard hydroxylamine-based processes.

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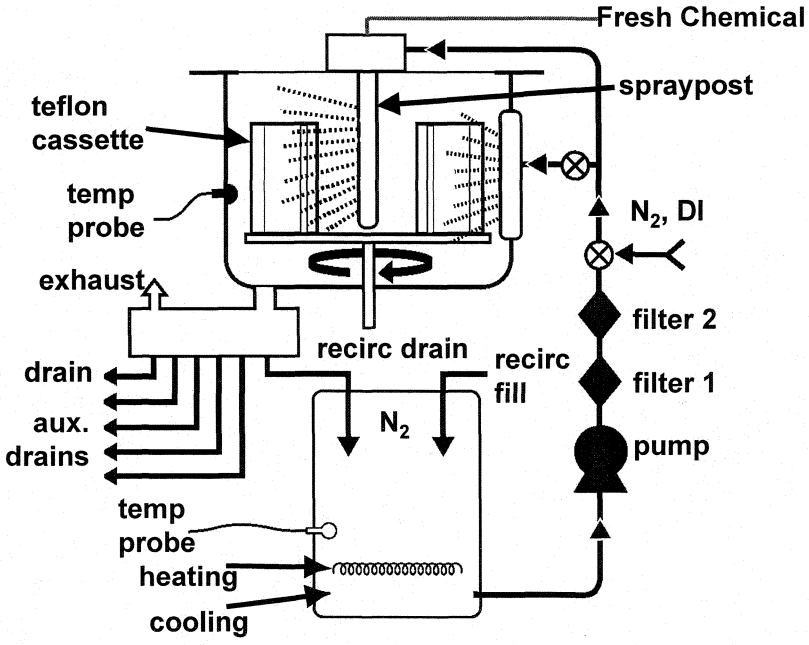

Figure 1. Spray Processor Configuration for RIE residue removal

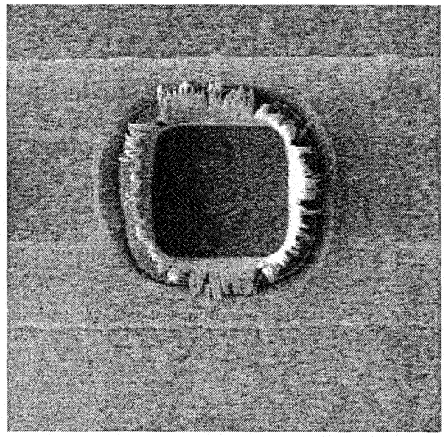

Figure 2. Initial condition after via etch and ash process

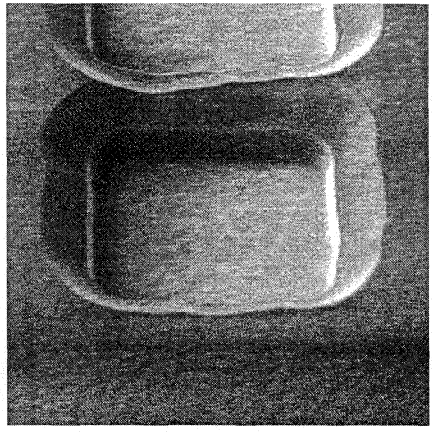

Figure 3. Dispense/rinse/dispense process

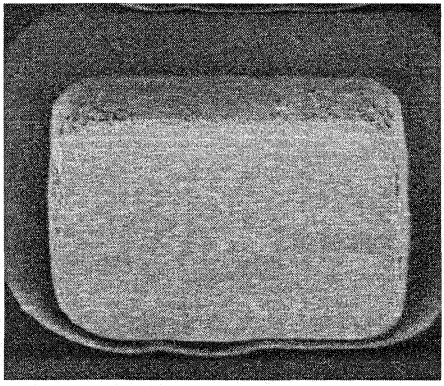

Figure 4. 5-min. one step dispense process

CORROSIVE BEHAVIOR OF TUNGSTEN IN POST-ETCH RESIDUE REMOVER

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Wet cleaning for resist strip and polymer removal has become more challenging with the continuous increases in density and number of interconnections and shrinkage of feature sizes in semiconductor industry. Tungsten (W)-plug via failure has become the main reliability issue in metal etching and post-etch cleaning due to the amine or hydroxylamine ingredients in the cleaning solution and chloride residues from chlorine-based etching process. The prevention of corrosion of tungsten plug requires understanding of the interaction between H^+ ions, chloride residue and the metal and also the effect of various process parameters such as processing temperature and photo resist stripping conditions. In our efforts to understand tungsten plug corrosion, the electrochemical behavior of W in EKC265 solution at room temperature and 65°C in the presence of DI water and/or Cl^- was investigated using Tafel curve, AC impedance measurement and scanning electron microscopy (SEM). The results show that Cl^- and DI water play very important role in enhancing the W corrosion. High PH value and temperature make the corrosion more severe, which is consistent with literature.

INTRODUCTION

Miniaturization of device features present on an integrated circuit, including isolation, gates, storage nodes, interconnects, and metallization, is essential for advanced device technologies. Each area is expected to continue reducing feature sizes, while maintaining or improving production yields. One of the device features is the tungsten plug which links the upper interconnects to the underlying layers, in particular, from the metal layers defining digit lines and periphery circuits to highly doped underlying silicon nodes. The fabrication of tungsten plug typically comprises the sequence of the pre-metal dielectric (PMD), deposition of Ti and TiN films, a rapid thermal anneal (RTA) and a CVD W deposition. The tungsten filled via plug process is commonly used in sub-0.5 μm CMOS process technologies, where it has been successfully implemented to provide aggressive contacted metal pitch. Increasing demands on the interconnect system to provide the

maximum density possible at the 0.25 μm and beyond device technologies require the overlaying metal pitch to be pushed to the limits of the lithography process. To achieve this in conjunction with low via resistance requires the metal-via overlap design rule to be reduced to zero. Such an approach called borderless contact, however, leads to unavoidable exposure of the tungsten filled vias due to misalignment and variation in critical dimension of the via and metal features (1, 2). When the tungsten plugs were exposed to hydroxylamine-based cleaning solutions, corrosion of the tungsten vias resulted (3, 4, 5). Figure 1 shows the corrosion originates at the tungsten that is exposed to the cleaning solution. Corroded tungsten vias led to the drastic increase in resistances and has become one of the key reliability issues for metal interconnects as feature size shrinks to 0.18 μm and beyond where zero-overlap design rule is applied (6).

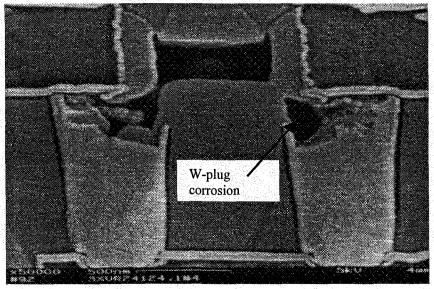

Figure 1. SEM micrographs shows the EOL (end-of-the-line) of a via chain cleaned in EKC265 solution during post-metal etch strip.

Undoubtedly knowledge of the electrochemical behavior of tungsten in the various cleaning solutions is critical to solve this corrosion problem and improve the device reliability. EKC265, which is a catechol-based alkaline solution, is one of the widely used post-etch residue strippers in semiconductor industry. Thus an attempt to study and investigate the corrosion behavior of tungsten in EKC265-based electrolytes was made and results are presented in this paper.

EXPERIMENTAL

Low-pressure chemical vapor deposited (LPCVD) tungsten film of approximately 0.4 μm thick was deposited over a Ti/TiN bilayer on 200 mm diameter silicon substrate. The tungsten deposited wafers were sliced into 1x1 cm samples for experiments. 0.1 M HCl and electronic grade DI water (resistivity 18 GΩ.cm) are used as additives for EKC265 so that the effect of chloride ion and DI water on tungsten corrosion can be investigated. A JEOL field emission scanning electron microscope (FESEM) was used to image the tungsten films. Open circuit potential (E_{corr}), Tafel and AC impedance measurements on tungsten films were performed on an EG&G Princeton Applied Research Model 273A

potentialstat/galvanostat interfaced to an EG&G model 5210EC lock-in-amplifier. All the electrochemical measurements were performed in the dark area. The electrochemical investigations were performed by using a glass flask with three separate necks for reference, counter and working electrodes and an inlet/outlet for water. Stoppers made of Teflon were used for each neck. The sliced tungsten sample was fitted onto a Teflon holder and held tightly between an O-ring leaving a surface of area 0.283 cm^2 exposed to the electrolytes. Electrochemical studies were carried out on tungsten films at room temperature subjected to the following conditions: (i) no treatment (reference); (ii) EKC265; (iii) EKC265:HCl (8:1 in volume); (iii) EKC265:DI water (1:1 in volume); (iv) EKC265:DI water(1:1):HCl. The same set of experiments were then repeated at 65°C because EKC265 is typically used at high temperature in the industry.

RESULTS AND DISCUSSION

Figure 2 shows the FESEM micrograph of the surface of CVD tungsten without any treatment. From the figure one can see the tungsten surface has a high degree of roughness due to grains with irregular sizes.

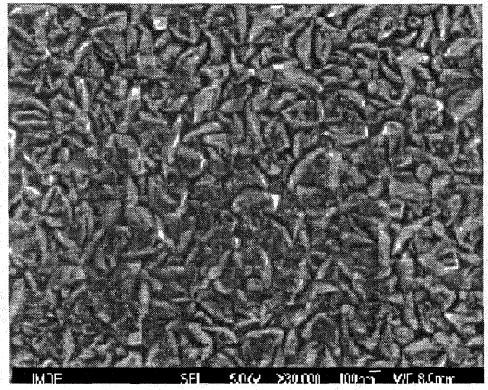

Figure 2. FESEM micrograph of the top surface of a CVD tungsten film taken at 30,000 times magnification

The first set of electrochemical experiments was done at room temperature and consisted of measuring the corrosion currents (Icorr) from Tafel plots and the charge transfer resistance (Rct) from AC impedance measurements. Figure 3 shows the Tafel plots for tungsten films exposed to pure EKC265 and EKC265 solutions added with DI water, 0.1M HCl and both DI water and 0.1M HCl. Figure 3 shows that the addition of HCl or DI water increases the corrosion rate of tungsten slightly and makes the open circuit potential (E_{corr}) less noble in the solutions. However, the addition of both HCl and

DI water raises the corrosion rate dramatically and shifts the E_{corr} to a much more negative value (-122.6 mV compared to –90.58 mV in pure EKC). Table 1 lists the corrosion current densities, E_{corr} determined by Tafel extrapolation and charge transfer resistance values from impedance measurements. The resistance values display an opposite trend with the corrosion current data. This is understandable since high charge transfer resistance meant less reactivity of the electrolytes and higher stability of tungsten in the solutions.

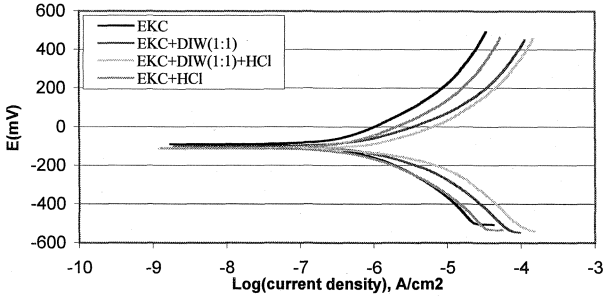

Figure 3. Tafel curves for CVD tungsten films in the absence or presence of DI water and HCl in EKC265 solutions at room temperature

Table 1. Tafel and charge transfer resistance data for CVD tungsten tested in EKC based electrolytes

Electrolytes	Icorr (uA/cm^2)	E_{corr} (mV)	Rct (KΩ)
EKC	0.6427	-90.58	90
EKC + HCl	0.7673	-109.1	84
EKC+H2O(1:1)	1.505	-100.3	16.5
EKC+H2O(1:1)+HCl	3.948	-122.6	14.6

The experiments were repeated at 65°C and the resulting Tafel plot is shown in Figure 4. It may be seen from the plots that the corrosion currents are higher than those measured at room temperature for all the four electrolytes. This shows that at high temperature the electrochemical reaction between tungsten and the electrolytes is accelerated and the corrosion is faster. We also find that the enhancing effects of HCl /DI water on tungsten corrosion are much more significant at 65°C than at room temperature. Addition of HCl or DI water increased the corrosion current by 4-5 fold. The corrosion current, E_{corr} and charge transfer resistance data at 65°C are tabulated in Table 2.

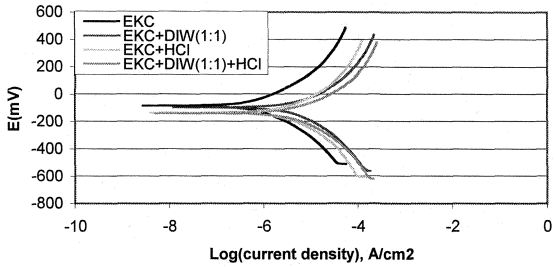

Figure 4. Tafel curves for CVD tungsten films in the absence or presence of DI water and HCl in EKC265 solutions at 65°C

Table 2. Tafel and charge transfer resistance data for CVD tungsten tested in EKC based Electrolytes

Electrolytes	Icorr, (A/cm^2)	E_{corr}, mV	Rp (KΩ)
EKC	0.884	-83.53	78.8
EKC + HCl	3.421	-134.6	21
EKC+H2O(1:1)	4.525	-97.04	18.7
EKC+H2O(1:1)+HCl	4.829	-138.1	11.9

Open circuit potential (Ecorr) is important in evaluating the corrosion behavior since it reflects the driving force of the corrosion reaction. The more negative Ecorr is, the metal is more prone to corrosion in the solutions. The E_{corr} data extrapolated from Tafel plots do not take into consideration the fact that E_{corr} will vary with time due to change of surface states of tungsten films after interacting with electrolytes. Thus the variation of E_{corr} vs. time in the four electrolytes at 65°C was monitored for 1 hour and the results were shown in Figure 5. It was observed that the E_{corr}s were strong functions of time in the early stage, which means the tungsten surface stage changed significantly due to dissolution or pitting formation. It is obvious that the E_{corr} were much more negative with the presence of HCl and /or DI water than that in EKC only. So tungsten is more prone to corrosion when DI water and HCl are present, which is consistent with the previous corrosion current data.

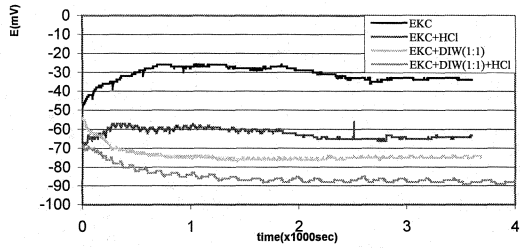

Figure 5. E_{corr} plot for W in EKC-based electrolytes at 65°C

To characterize the surface changes of tungsten films after treatment in EKC-based electrolytes and study the tungsten removal mechanism in these electrolytes, the samples were characterized by FESEM (Figure 6 (a)-(d)). When compared to the surface morphology before treatment (Figure 2), Fig 6(a) and 6(b) did not show significant difference and the grains can be clearly seen. This may suggest that tungsten was removed layer by layer. However, in Fig 6(c) it can be seen that the grain structures are distorted. After treatment in EKC together with DI water and HCl, total morphological change and corrosion pits are observed (Fig 6(d)). These results show there is area/volume loss of W owing to surface reaction with cleaning solution. There is also localized corrosion (pitting) owing to higher surface energy. The mechanism is a combination of surface removal plus pitting when HCl and DI water are present.

CONCLUSION

The electrochemical behavior of tungsten in EKC265 containing HCl or/and DI water was investigated to elucidate the effect of HCl and DI water on tungsten dissolution in the cleaning solutions. The electrochemical data obtained using different electrolytes at different temperature were compared. These data include Tafel plots, ac impedance spectra, E_{corr} plots and FESEM characterization. Addition of HCl and DI water increased the corrosion current and made E_{corr} more negative. So, HCl and DI water significantly enhance the W corrosion. High temperature enhanced the electrochemical reaction. Thus operation at room temperature is suggested. It was concluded that the W removal mechanism in EKC was a combination of pitting and bulk removal based on the FESEM data.

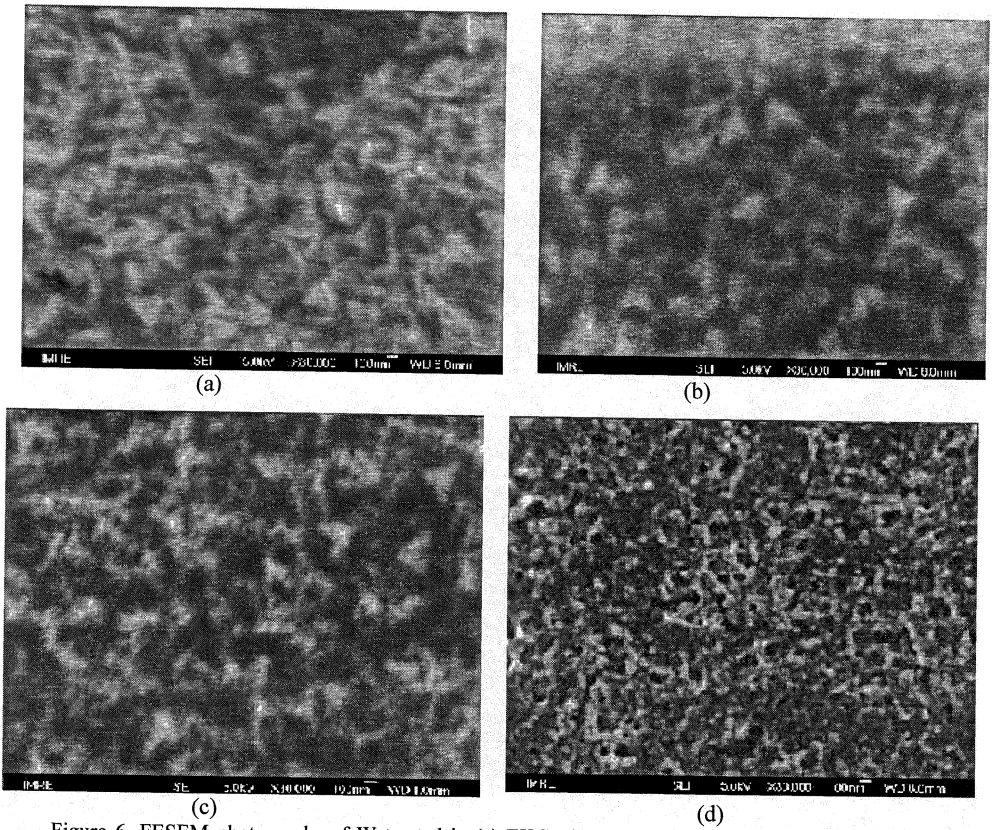

Figure 6. FESEM photographs of W treated in (a) EKC; (b) EKC+DI water (1:1); (c) EKC + HCl; (d) EKC+DI water (1:1)+HCl

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EMERGING TECHNOLOGIES

EFFECTS OF SUPERCRITICAL CO_2 ON THE ELECTRICAL CHARACTERISTICS OF SEMICONDUCTOR DEVICES

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Despite implementation and cost constraints of high pressure equipment, supercritical carbon dioxide is becoming one of the most attractive substitutes for chlorinated and CFC solvents, volatile organic compound (VOC's) and RCA based chemistries which are currently used in the semiconductor industry.
In this study the effects of supercritical fluid conditions of temperature and pressure on the electrical properties of various devices have been investigated. No difference was observed in the properties of the devices before and after treatment in supercritical carbon dioxide.

INTRODUCTION

Wafer cleaning is a significant contributor to the cost of ownership of IC manufacturing. In fact wafer cleaning now comprises of about 30% of all process steps, since cleaning of wafers must take place after each major processing step and before each high temperature operation.

In all cleaning applications, the increasing demand is for greater efficiency and effectiveness in contaminant removal. There is a market drive for environmentally conscious semiconductor and electronic parts cleaning. In particular due to aggressive scheduling imposed by legislative bodies, there is a requirement to phase out the production and use of ozone-depleting substances such as CFCs and a reduction in volatile organic compounds (VOC) emissions from of organic solvents use. In addition, reducing worker exposure to VOC's has also become increasingly important in the electronic industry. Existing cleaning processes available to the industry e.g. RCA (wet chemical) based cleans for semiconductors [1], flux cleaning for oxides in semiconductor devices and solvent cleaning of flux residues in electronic systems, are limited in their environmental capabilities. In particular these cleans generate large volumes of waste solvents, increase worker exposure to solvents, and require costly chemicals and expensive equipment. As such, there is a requirement for the development and integration of a closed loop, environmentally and substrate compatible, cost effective technology resulting in significant savings in solvent and associated energy costs. The use of supercritical fluids in cleaning applications is one such solution.

Supercritical fluids act with the properties of a liquid and a gas. This can be explained by reference to Fig 1. which is a phase diagram for carbon dioxide. In the diagram we

can see the areas where the substance exists as a solid, liquid or gas. The curves represent coexistence between two of the phases. The vapour pressure (boiling) starts at the triple point (TP) and ends at the critical point (CP). The critical region has its origin at the critical point. We can therefore define a *supercritical fluid* as any substance that is above its critical temperature (Tc) and critical pressure (Pc).

Figure 2 illustrates the disappearance in distinction between the liquid and gas phases as the substance approaches the critical point in a given cell volume. Shown in the diagram are three schematic representations of a view cell in which the experiment is conducted at appropriate points on the gas-liquid coexistence curve. Cell *a* is at the lowest temperature with the meniscus between the gas and liquid phase being quite distinct. As the temperature and pressure are increased, the density difference between the two phases reduces and the meniscus becomes less distinct (cell *b*). When the critical point has been passed the meniscus disappears altogether as shown in cell c.

Naturally occurring carbon dioxide gas, which in its supercritical state, acts as a powerful solvent , can penetrate just about everywhere. Carbon dioxide gas is inexpensive, recyclable, and is environmentally benign. Although it is a greenhouse gas it is not a net addition as it is obtained in large quantities as a by-product of fermentation, combustion and ammonia synthesis and would eventually be released into the atmosphere if it was not used in as a supercritical fluid. Other advantages are that it is not considered to be a volatile organic compound, an ozone-depleting compound, a hazardous air pollutant (HAP) nor is it flammable.

Supercritical fluids are in widespread use across many industries - the food industry uses supercritical fluids to decaffeinate coffee and to extract the flavoring of hops for beer; the textile industry uses supercritical fluids to clean materials and garments; and waste treatment firms use supercritical fluid for advanced hazardous waste extraction and nuclear waste management.

Recent work on supercritical fluids indicate that as well as successively removing organic contaminants, the technology may also be used to remove or extract metals by using metal complexing ligands.[3] These discoveries open the potential for a multi-purpose (organic and metallic or ionic contaminant removal) cleaning process which is compatible with environmentally conscious manufacturing and the process requirements of contaminant-sensitive materials and form the basic innovation of this work.

In the past few years a number of research groups have been investigating the use of supercritical fluids for various cleaning applications in the electronics industry. There are already a number of commercially available instruments for supercritical fluid drying of MEMS devices and there is also some work being done on particle and photoresist removal from semiconductor wafers. [4],[5].

EXPERIMENTAL DETAILS

A test chip for a 15 volt, 5μm CMOS process, which is capable of evaluating the impact of process steps on contacts, gate oxide integrity, diode leakage, field device leakage, line-width, contact resistance, inter layer and intra layer isolation, electromigration, transistors, capacitors and resistors was used in this work. This device was used to evaluate the impact of supercritical carbon dioxide cleaning process on these parameters.

This device was fabricated in wafer form and evaluated after passivation. Each wafer contained approximately 60 process monitoring chips.

The electrical characteristics of each wafer were first determined using the measurement setup shown in Fig 3 and wafer maps were generated for each wafer and each of the parameters shown below. These parameters were measured for both n and p devices.

- P- and n-channel transistors of various W/L
  These transistors have common source, gate and bulk connectors.
  The following parameters were tested: Vt, maximum transconductance, gate current, drain current and substrate current.
- Different sized pn junctions were used to measure source/drain leakage current along the field oxide edge.
- Metal-poly isolation resistance
- Gate oxide monitor structures
  The objective is to measure the integrity of the gate oxide in the gate oxide planar region. This is achieved by maximizing the gate oxide planar area and creating a large gate oxide capacitor using polysilicon and metal as the top plate. Breakdown voltage of the gate material is used as a measurement of the quality of the gate oxide.

A simplified schematic of the supercritical fluid instrument used in these experiments is shown in figure 4. It consists of a storage vessel for the carbon dioxide, a syringe pump, an extraction vessel housed in an oven, a pressure control valve and a collection vessel for any extracted components. In this case the carbon dioxide was vented to the atmosphere as nothing was extracted.

Following device fabrication, the wafers were placed in the extraction vessel and then subjected to various conditions of time, temperature and pressure as shown in the graphs in figure 5. The highest pressure used was 200bar and the highest temperature used was 80°C.

Finally the same electrical tests as before were then carried out on the wafers and wafer maps were generated for 19 different electrical parameters for each chip.
The goal of this experiment was to see if any of the parameters had significantly increased or decreased resulting in chip failure and to determine the effect of the various supercritical fluid conditions on the performance of the devices.

RESULTS AND DISCUSSION

Six wafer maps are shown in figure 6. They show three wafers before and the same three wafers after supercritical fluid processing. The first two wafer maps , (1a) and (1b), give measurements of Vt for a p-channel transistor before and after the supercritical fluid process (A) in Fig.5. The second two wafer maps, (2a) and (2b), give measurements of the leakage capacitor voltage applied to an n-channel device at breakdown before and after supercritical fluid process (C). This provides a measurement of the gate oxide integrity. The third pair of wafer maps, (3a) and (3b), give the leakage current values for a p+n diode before and after supercritical fluid process (D).

As can be seen from the wafer maps, there is no observable difference between the devices after treatment in supercritical carbon dioxide. Although space constraints prevent inclusion of wafer maps for the other electrical characteristics mentioned in the previous section, results have shown that neither of the four supercritical fluid processing steps used affected these values.

CONCLUSION

Preliminary results indicate that CO_2 based supercritical fluids have no measurable effect on silicon microelectronic structures and therefore it can be assumed that these devices can be cleaned using supercritical carbon dioxide without a reduction in yield.
This is a good indication to commence further work on supercritical fluid cleaning technologies as a substitute for the typical cleans used in semiconductor manufacturing. In particular, such processes as pre oxidation cleans, resist stripping and pre metal deposition. Cleans could possibly strongly benefit from this technique. Finally the environmental benefit and cost savings of supercritical fluid processing would be substantial.

ACKNOWLEDGMENTS

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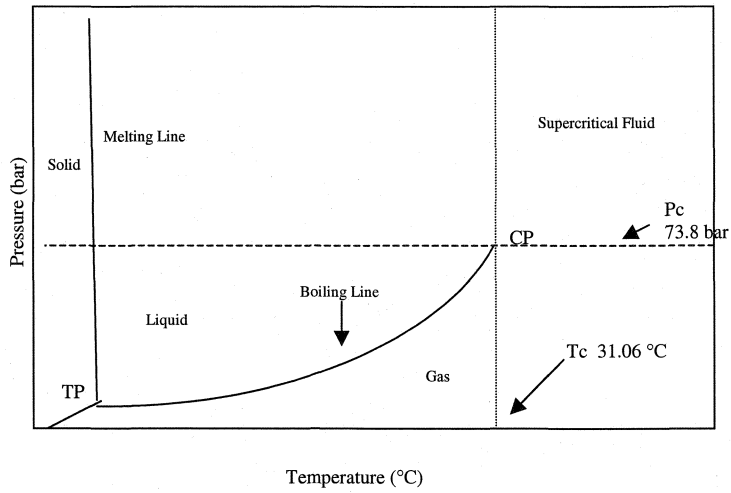

Fig 1. Phase (pressure-temperature) diagram for CO_2: TP = Triple Point, CP = Critical Point, Tc = critical temperature, Pc = critical pressure

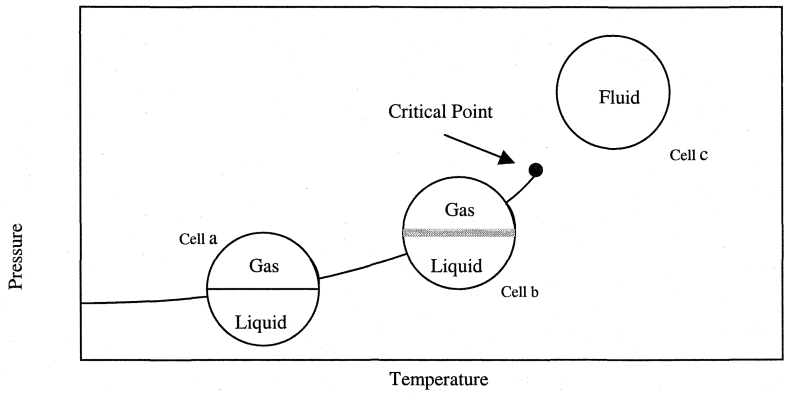

Fig 2. Disappearance of the meniscus at the critical point [2]

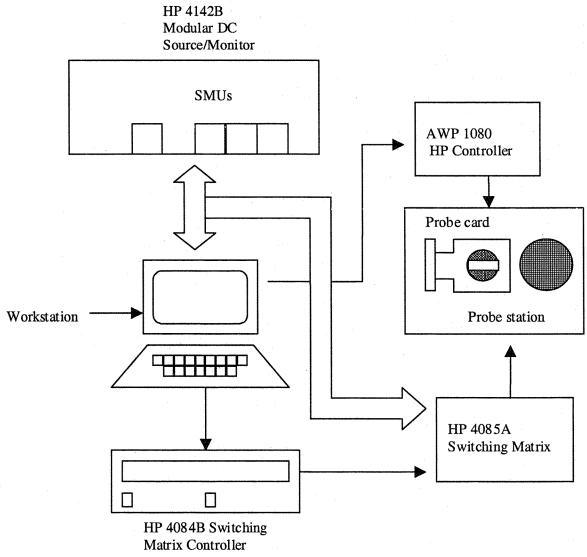

Fig 3. : Automatic DC measurement setup.

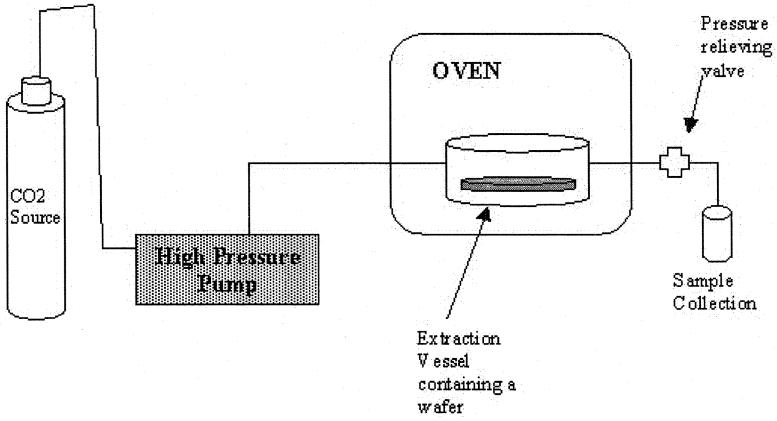

Fig 4.: Supercritical fluid instrumentation setup

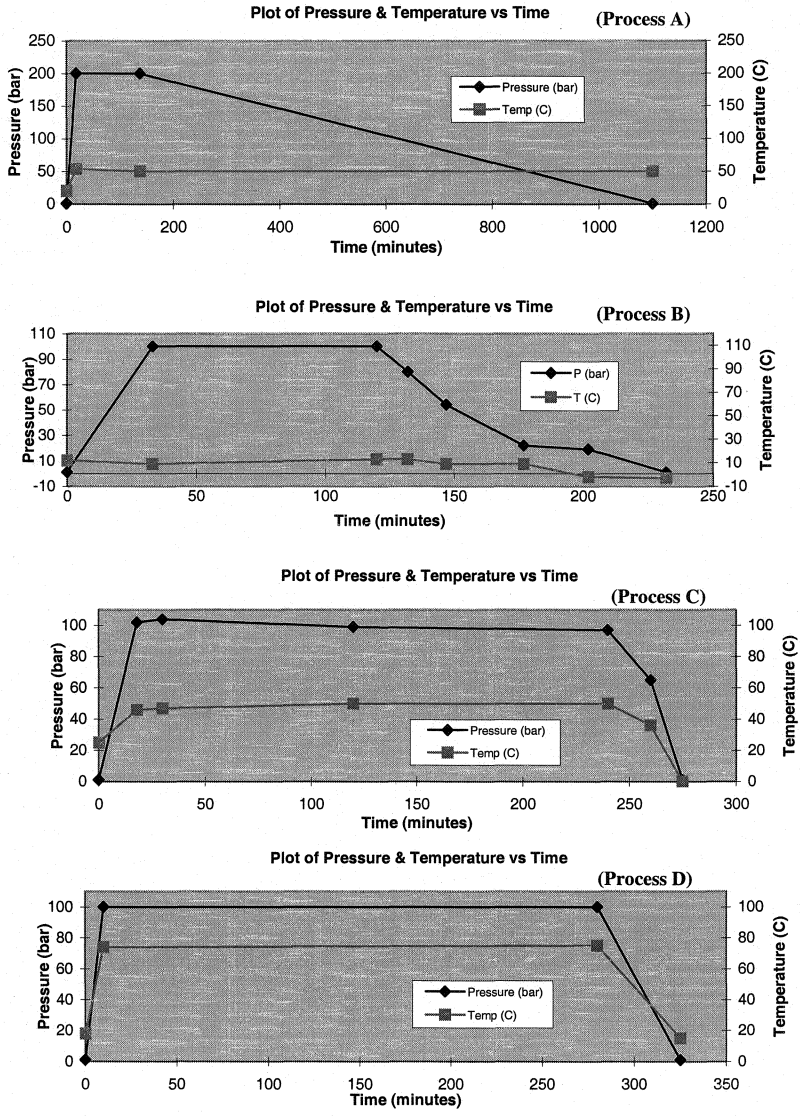

Fig 5.Experimental conditions of temp. and pressure for wafers 1-4 (process A-D)

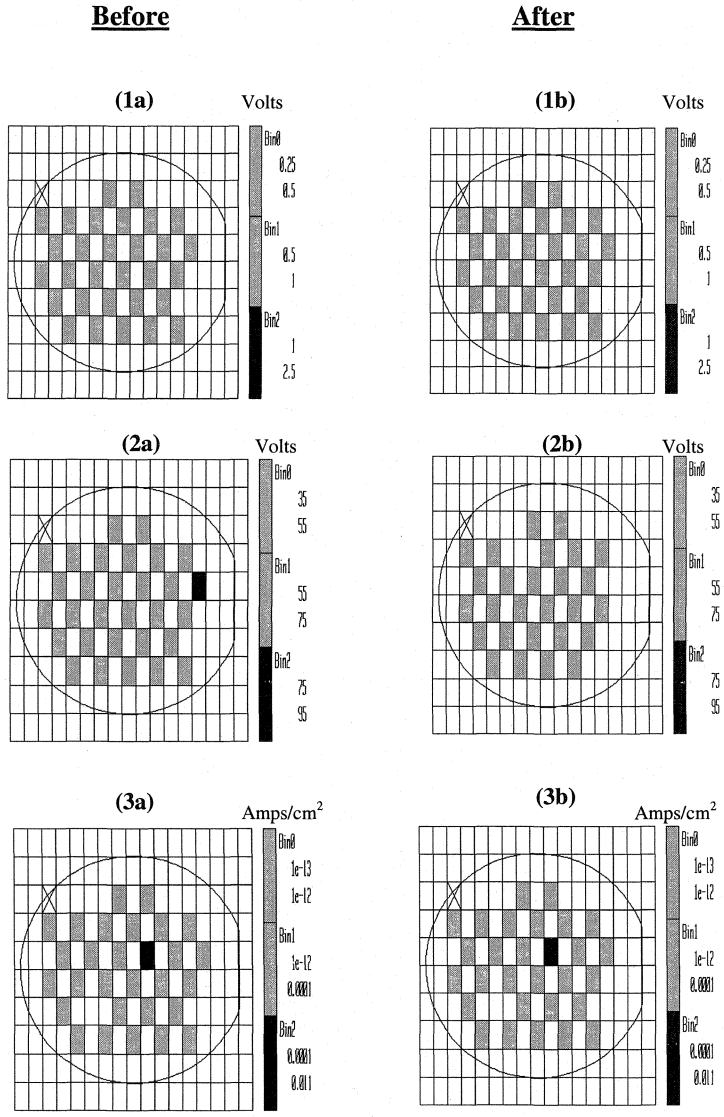

Fig. 6. : Wafer maps for wafers before and after supercritical fluid processing

OZONATED HF APPLICATIONS IN A SPRAY PROCESSING TOOL

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A HydrOzone™ process combined with an ozone-HF step, applied in a spray-processing tool, is feasible in removing both resist and post-etch polymer residues after polysilicon etch on CMOS and NVM wafers. With this method, the chemical use and process time are reduced significantly. In addition, this HydrOzone™ process extended with an ozone-HF step provides an effective comprehensive pre-gate clean with no significant adverse impact of surface roughness on the gate oxide properties.

INTRODUCTION

With dimensions scaling down, more polymerizing chemistries (such as hydrogen bromide (HBr)) for polysilicon etch are necessary to obtain a better selectivity towards the gate oxide. This also implies difficulties in polymer removal after etch. Frequently, HF and SC1-based wet chemistries are used in combination with oxidative chemistries for the removal of polysilicon etch residues (including resist layers) (1), (2). Initial experience indicates that HydrOzone™ (3), i.e. mixture of ozone/DIwater, is feasible for resist removal, however the etch (and ash) polymers are more resistant. Development of a wet process based on HydrOzone™ for removal of etch polymers would be effective from a cost, environmental and throughput point of view. This is realized for standard CMOS and NVM (non-volatile memory) processes by extending the HydrOzone™ method with an additional step containing a mixture of ozone and diluted HF.

The ozone-HF extended HydrOzone™ process also shows potential for pre-gate clean applications in a spray-processing tool (4), (5), (6). The performance of this clean in terms of oxide, organic contamination, particle and metal removal was previously investigated (4). Additional experiments on particle removal efficiency, wafer surface roughness and electrical characterization will be described in this paper.

EXPERIMENTAL

Strip after polysilicon etch was performed on CMOS wafers (8", p-type, Cz, <100>) with a standard C025 poly/gate (250 nm/5 nm thickness) stack deposition. Deep

Ultraviolet (DUV) photoresist and a bottom antireflective coating (BARC) are used for patterning. Strip after NVM poly etching was done on 8 inch wafers, which got a 250 nm poly on top of a 100 nm thermal oxide followed by a non critical I-line print (C035). Etching chemistries comprises a combination of HBr and oxygen (BARC etch), followed by chlorine, hydrogen bromide and oxygen (main etch) and finally HBr for over-etching. After etch, both wafer types were exposed either to an IMEC standard strip (served as reference), a HydrOzone™ strip with NH_4OH as additive or HydrOzone™ strip followed by an ozone-HF step. The IMEC standard strip (ca. 20') features an ammonium hydroxide peroxide step (70°C) followed by a sulfuric acid/peroxide mixture (SPM) at 90°C. The HydrOzone™ (ozone (185 g/m^3, 10 lpm) and DIwater (5 lpm)) strip for CMOS wafers is performed for about 6' at 85°C and high rotational speed (800 RPM) with NH_4OH (1/2500) as additive. Previous experience showed a higher removal efficiency of resist/polymers if additives are used during ozonated processes (3). The new strip sequentially processes wafers, first through HydrOzone™ (6 minutes for CMOS and 8 minutes for NVM) and then through an ozone-HF (1.5 minutes for CMOS and 8 minutes for NVM) step at low rotational speed (50 RPM). A HF concentration of approximately 0.1%(v/v), an ozone concentration of 185 g/m^3 and a working temperature of 95°C are defined as the standard ozone-HF process. At high temperatures, a better particle removal efficiency was observed (5). The combined process steps are sequentially performed in the same chamber of a spray-processing tool. Ozone and HF/water are separately inserted in the process chamber. Ozone concentrations are monitored by means of a BMT 963 ozone analyzer.

Cleanliness was inspected with a Scanning Electron Microscope (PHILIPS SEM XL 30). After stripping, the charge (Q) to break down (Q_{BD}) and transistor parameters were investigated on a C025 integration lot.

Pre-gate clean capabilities, more specifically particle removal, surface roughness and electrical parameters, of the combined process were also investigated on p-type silicon wafers. For this purpose, both the HydrOzone™ (2 min.) and ozone-HF (4 min.) step operate at a low rotational speed of 50 RPM. Si_3N_4 and silica slurry (SiO_2) particle removal on bare silicon and thermal oxide (500 nm) was studied using an immersion based controlled contamination procedure, followed by rinse and dry. Approximately, 30,000 and 6,000 Si_3N_4 particles were deposited on bare silicon and thermal oxide wafers, respectively. Around 10,000 SiO_2 particles were deposited on both bare and thermal oxide wafers. The LPD levels were measured with a KLA Tencor SP1-TBI tool in dark field wide oblique (DWO) detection mode from 0.12 µm size on. Wafer surface roughness was determined with atomic force microscopy (AFM, Nanoscope III dimension 3000) scans over 1 µm length. Field (E) dependent break down (E_{BD}) was performed on three sizes of capacitors (9.7, 2.8, 0.9 mm^2).

RESULTS AND DISCUSSION

Strip after polysilicon etch

Polysilicon stripping in ozone-HF solutions is a simultaneous process of poly oxidation and poly-oxide etching. Preceding experiments have shown that this is a competition process between the oxidation and etching reaction (7). The slowest reactions would be the rate-limiting step and determines the overall poly etching kinetics. The objective is to maintain hydrophilic surfaces during processing and thus low HF (0.1%) concentrations and high ozone concentrations (185 g/m^3 O_3) are applied. Under these conditions, polysilicon is not significantly etched.

The novel process, HydrOzone™ followed by ozone-HF, is demonstrated for cleaning post-etch polymer residues after polysilicon etch. Figure 1 shows SEM pictures of CMOS structures after a conventional and ozone-HF extended HydrOzone™ treatment. The ozone HF extended HydrOzone™ process is able to remove both resist and polymers, while with the conventional HydrOzone™ strip, applying NH_4OH, polymers still remain on the structures and the surface. The HydrOzone™ step at high rotational speed (800 RPM) removes the resist layer but not the polymers or polymer-etch residues. To remove these polymers, an additional step, using ozone-HF, is used at a low rotational speed (50 RPM). In this way, a thicker boundary layer is present on the wafer and thus the polymer etch residues are restrained to re-adsorb on the wafer surface. Therefore, formation of polymer clusters does not occur. Also, at low rotational speed a longer contact time of the solution with the polymers on the wafer exists.

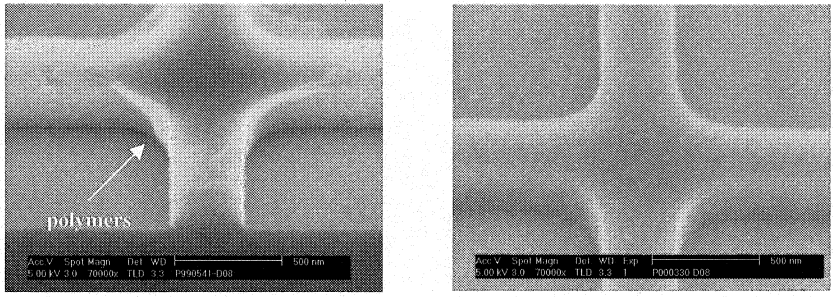

Figure 1: SEM photographs of a CMOS structure after a conventional HydrOzone™ strip with NH_4OH (left) and a HydrOzone™ strip extended with ozone-HF (right).

For NVM processing, more highly polymerizing etch chemistries are used compared to CMOS processing. Therefore, slightly longer process times are needed to remove resist and polymer-etch residues. Results are depicted in Figure 2. With a conventional HydrOzone™ clean applying NH_4OH, the resist could even not be completely removed.

However, extending the same clean with an ozone-HF step shows enormous enhancement achieved; both resist and post-etch polymer residues are stripped.

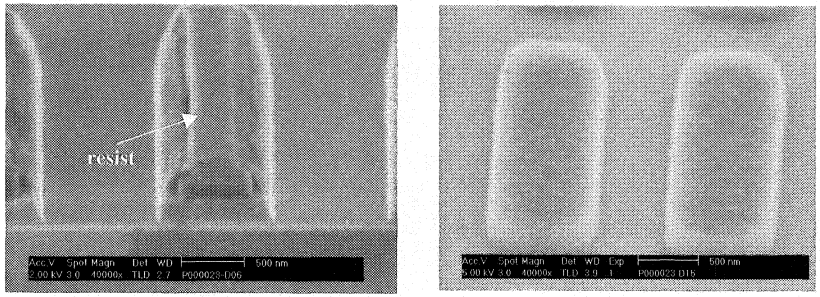

Figure 2. SEM photographs of a NVM structure after a HydrOzone™ strip with NH_4OH (left) and a HydrOzone™ strip extended with ozone-HF (right).

Electrical characterization of capacitors and transistors is also investigated. If any influence of strip after polysilicon etch is expected on the quality of the gate oxide, the non-overlapping meander capacitor will be the most sensitive. The current density used for measurements is 2000 A/m^2. A Weibull plot of large meander n-well and p-well capacitors is represented in Figure 3. In order to calculate the parameter F (median rank), the Q_{BD} data are sorted from low to high. After that, each Q_{BD} value is given a rank (starting from 1 to ...). F is then defined by (Rank - 0.3)/(Total number of data + 0.4). No significant differences were seen between the IMEC standard and the ozone-HF extended HydrOzone™ strip, based on the measurement of 26 dies on each wafer.

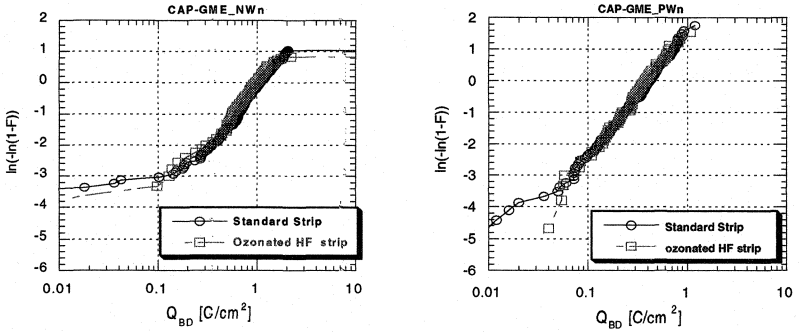

Figure 3. Q_{BD} distribution for standard IMEC strip and HydrOzone™ extended with ozone-HF strip on n-well (left) and p-well (right) capacitors. (CAP: capacitor; GME:meander; NWn: n-well poly non-overlapping on field).

No influence of the strip after polysilicon etch was seen on the intrinsic transistor performance (both NMOS (not shown) and PMOS); see Figure 4 (left side). Figure 4 (right side) shows the threshold voltage rolloff (i.e. threshold voltage as function of device length) independency of the strip after poly etch on NMOS transistors.

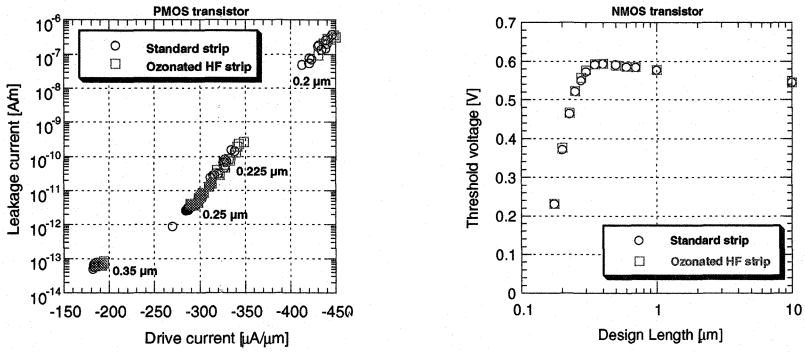

Figure 4. Leakage current versus drive current for different transistor lengths on PMOS (left) and threshold voltage as function of device length on NMOS (right) transistors after standard IMEC strip and HydrOzone™ extended with ozone-HF strip.

Pre-gate clean

Previously, cleaning capability of this clean in terms of etch rate/uniformity, organic contamination, particle and metal removal efficiency were already investigated (4). Additional information on nitride particle removal efficiency, roughness and electrical characterization is given below.

In this study, Si_3N_4 and SiO_2 particles removal efficiency on bare silicon and thermal oxide (500 nm) wafers are determined. Results are given in Figure 5 (left). SiO_2 particles are easily removed on thermal oxide (96%) wafers as well as on bare silicon wafers (99.8 %). The removal efficiency of nitride particles on thermal oxide is around 99.4%. However, results are somewhat erratic, with removal efficiency of around 40%, for silicon nitride particles on bare silicon substrates. Probably, the nitride particles are somehow modified after the ozone-HF process and therefore more difficult to remove from the bare silicon surface. This problem is also observed in other processes using ozone de-ionized water (8). When the ozone supply in the ozone-HF step is intermittenly cycled on and off (9) during the course of the cleaning step, cleaning efficiency increased to > 99% (6).

To investigate silicon surface roughening by the ozone-HF process described in this study, bare silicon as well as epitaxial (EPI, more sensitive towards surface roughness)

wafers are exposed for 4 minutes to ozone-HF and compared with IMEC cleaned (10) control wafers. Results are depicted in Figure 5 (right hand side).

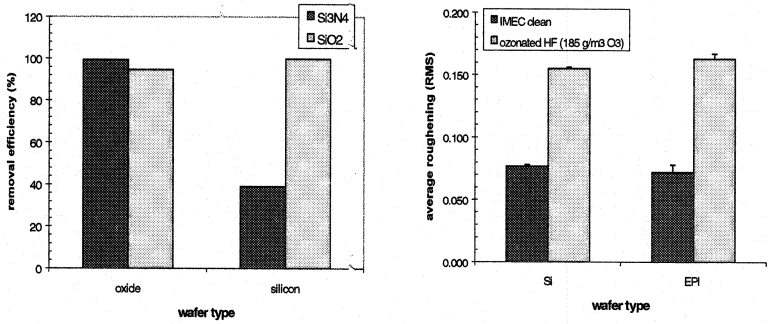

Figure 5. (Left) Removal efficiency of Si_3N_4 and SiO_2 on bare silicon and thermal oxide wafers after a HydrOzone™ process extended with an ozone-HF step and (Right) average roughness (nm RMS) on Si and EPI wafers after different cleans, measured with AFM (right).

On both EPI and bare silicon wafers, an increase (~ 0.7 Å RMS) in surface roughness is observed when wafers are exposed to the ozone-HF process. In principle, if the balance between oxidation/etching is lost and etching predominates, micro-roughness increases. This increase is more pronounced when the starting wafer surface roughness is lower than 0.1 nm RMS. For a starting surface roughness >0.1 nm RMS, no significant increase is seen after an ozone-HF treatment (6).

The impact of increased roughness on the dielectric breakdown is experimentally verified. P-type silicon surfaces were exposed to different cleans, where after a 5 nm/250 nm gate oxide/polySi stack was deposited. Ramped voltage stress (e- injection through poly) is used for evaluating the gate oxide integrity (GOI) on 84 capacitors from 3 different sizes. The intrinsic E_{BD} yield is defined as the fraction of capacitors that survives a field stress of 12 MV/cm over the gate oxide (i.e. 7 V over the entire capacitor). Figure 6 contains ramped voltage E_{BD} area yield results from p type wafers as function of pre-gate clean. For the ozonated HF clean, a few break downs (4%) are observed in low field (< 2 MV/cm) and mid field area (between 2 and 12 MV/cm), while for the IMEC clean a mid field yield of only 3% is observed. Consequently, the intrinsic E_{BD} yield for the ozonated HF and IMEC clean amounts 92% and 97%, respectively. On small capacitors (2.8 and 0.9 mm^2), an E_{BD} yield of 100 % is obtained for all cleans under study (not shown). Hence, no significant adverse impact of surface roughness on device performance is observed. This is in conformity with previous results showing that moderate roughness (i.e. < 0.4 nm RMS) does not have an influence on the current

voltage characteristics and charge-to-breakdown distributions of MOS capacitor structures with ultra-thin SiO_2 layers (11), (12).
Note, that for transistors, a surface roughness of around 0.3 nm RMS already causes a decrease in electron channel mobility (13). Therefore, transistor parameters still need to be checked for this type of clean.

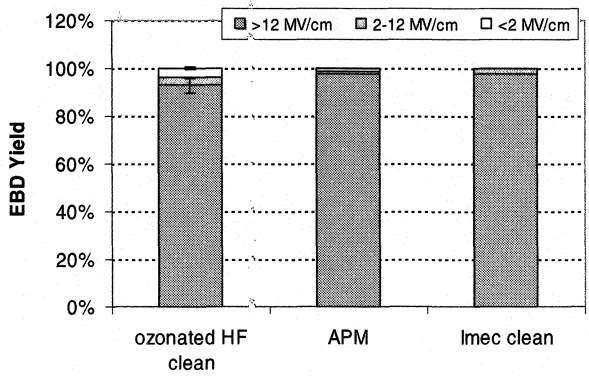

Figure 6. The 5 nm thick oxide E_{BD} yield as function of applied voltage for different pre-gate cleans (Capacitor area is 9.7 mm^2 and 84 capacitors tested).

CONCLUSIONS

An ozone-HF process, applied in a spray-processing tool is feasible in removing both resist and post-etch polymer residues after polysilicon etch, without influencing the gate oxide properties. Compared to standard strip procedures, both the chemical use and process time are reduced significantly. Furthermore, this process can be used as an effective comprehensive pre-gate clean with no significant adverse impact of surface roughness on the gate oxide properties. However, the effect on transistor parameters still needs to be investigated.

ACKNOWLEDGEMENT

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THE EFFECT OF SURFACTANTS IN DILUTE HF SOLUTIONS

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The effect of adding surfactants to dilute-HF containing solutions was investigated. It was determined that surfactants have an impact on particle and metals levels and may consequently affect properties such as minority carrier lifetime and thermal oxide thickness. The results also indicate that wafer particulate levels on bare silicon wafers decrease upon thermal oxide growth. Other parameters such as surface micro roughness, interface trap density and breakdown voltage have also been studied.

INTRODUCTION

Dilute hydrofluoric acid (DHF) is used in etching, stripping and cleaning thin silicon dioxide (<500 Å) films. Although diluted HF is employed to decrease the etch rate it is not as controllable in thick oxides since hydrogen ions generated during the reaction of silicon with HF readily adsorb onto the silicon surface leading to non-uniform etching through micromasking [1]. However, the use of diluted hydrofluoric acid as a cleaning solution and moreover as a primary etchant for thin gate oxides has gained widespread use [2-3]. In addition, the incorporation of surfactants has been recently introduced since they have been employed to improve surface wetting and etch uniformity [4], porous silicon [5-6] properties, and to reduce particulate and trace metals contamination after cleaning [7]. This study examines commercially available surfactanated dilute HF effects on cleaning, oxide properties and electrical behavior.

EXPERIMENTAL

Prime 100-mm p-type silicon wafers were immersed sequentially in a modified RCA-1 followed by RCA-2 and finally in dilute HF (100:1) containing different surfactants. The table below provides the general composition of the surfactants present in dilute HF.

Table 1. Surfactanated Dilute HF Compositions

Group	Surfactant type
A	Fluorosurfactant 1
B	amine/alcohol co-surfactant 1
C	Fluorosurfactant 2
D	Alcohol/amine co-surfactant 2

Metal and particle contamination levels were monitored prior to and following a nominal 170 Å thermal oxide growth. Surface metallics were identified using Total Reflection X-ray Spectrometry (TXRF), while particles on wafers were quantified by laser scattering. Oxide thickness was measured using ellipsometry. Surface roughness was determined using Atomic Force Microscopy (AFM). A surface charge analyzer (SCA) was utilized to determine minority carrier lifetime and interface trap density of oxidized wafers. Aluminum gate MOS capacitors were fabricated and used in a voltage ramp test to determine dielectric breakdown strength. A control group processed identically with the dilute HF groups, but without the surfactant was included for comparison testing.

RESULTS

After immersion in dilute HF, iron levels were most elevated for Group B wafers as shown in Figure 1.

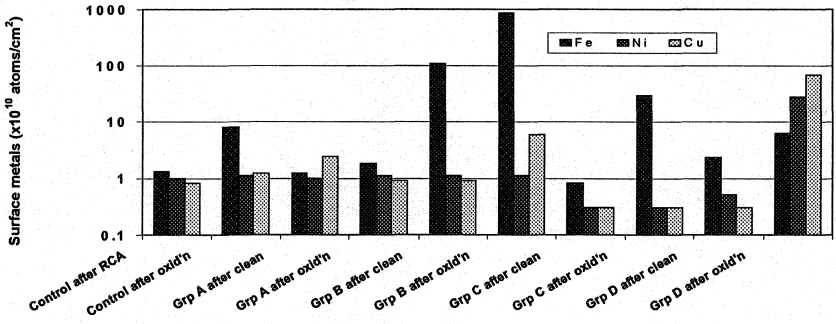

Figure 1. Wafer surface trace metal by TXRF

Certain wafer surface trace metal impurities exhibit opposite trends after dilute HF clean and thermal oxidation. TXRF analysis indicates that iron levels increase following oxide growth. On the other hand, copper levels vary with different surfactants, which is consistent with mixed results from earlier studies [4,8-9]. Although surfactants in Group A and C, and Group B and D share similar chemical nature, the surface metallic contributions can vary widely. As shown in Figure 2, particles were also most elevated wafers for Group B after immersion in a dilute HF with surfactant.

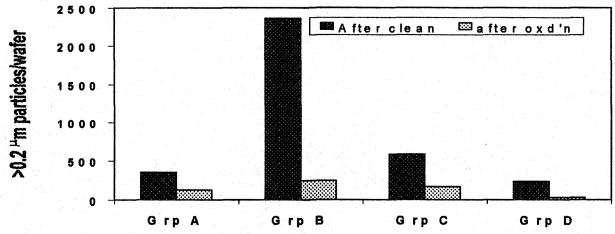

Figure 2. Particles on wafers

Particulate levels also decreased following thermal oxide growth for most groups. The effect is most pronounced with Group B. Figure 3 reveals that a significantly thicker oxide is grown with Group B wafers. Group A oxide thickness is similar to the control group while Group C and D oxides approach the targeted 170 Å thickness.

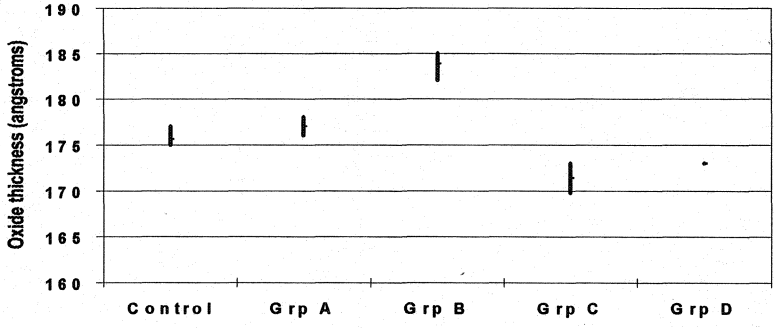

Figure 3. Thermal oxide thickness

In addition, the electrical characterization of the thermal oxide indicates reduced minority carrier lifetime associated with Group B wafers as shown in Figure 4.

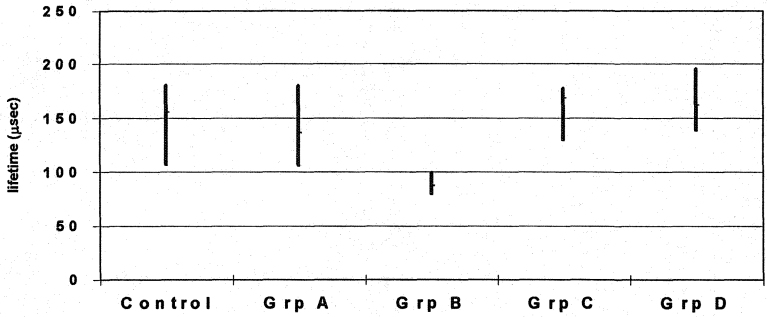

Figure 4. Minority carrier lifetime

Other electrical and physical parameters such as interface trap density (D_{it}), oxide breakdown voltage (V_{BD}) and surface micro roughness have been investigated and the results tabulated.

Table 2. Electrical Testing and AFM Data

Test	Cntrl	Grp A	Grp B	Grp C	Grp D
Interface trap density, D_{it} (xE11/eV-cm^2)	0.95	1.16	1.65	0.99	0.96
µroughness, Ra (Å)	1.2	1.2	1.1	1.2	1.2
RMS (Å)	1.5	1.6	1.4	1.5	1.5
Breakdown Voltage, V_{BD} median (MV/cm)	10	9.8	9.8	9	9.7

No major differences are observed in surface micro roughness for various surfactanated hydrofluoric acid solutions although earlier studies indicated that other types of surfactants assist in minimizing surface roughness [4]. However, the interface trap density, which is an indirect indicator of surface microroughness is most notable for Group B.

Metal-on-semiconductor (MOS) aluminum capacitors were also built and tested for oxide breakdown. Again, no significant differences were observed between the test groups. The mean values of the dies tested shown to be at or above 9 MV/cm.

DISCUSSION

Only lifetime, particles and high trace metals, particularly iron appear to be significant for the various surfactanated dilute HF solutions tested. The reduced lifetime may be the

result of higher iron concentration at above 10^{12} atoms/cm^2 found on bare silicon. However, an attempt to compare the iron levels on silicon vs. iron analyzed in the surfactanated solution shows no clear correlation as shown in the following table.

Table 3. Iron levels

	Cntrl	Grp A	Grp B	Grp C	Grp D
Surface Fe ($x10^{10}$ at/cm^2)	1.6	1.2	106	0.8	2.3
Solution Fe (ppb)	<1	13	10	<1	4

Interestingly, while Group A and Group B have similar iron levels in their respective HF solutions, the deposition amount can vary over two orders of magnitude. Several authors eluded to an interaction between surfactants and silicon wafer prevent deposition of metallic contaminants [2,4]. On the other hand, it may also be possible that surfactants complexate or bind with the free metallic ion. Lifetime degradation is typically associated with iron thermally diffusing into bulk silicon. It also appears from the data above that the iron in the oxide film and bare silicon stems from two potentially different sources. The iron found in the oxide is more likely the result of additional contamination from the oxidation furnace.

Another interesting finding was that Group B wafers exhibited particle patterns detected using the wafer laser scattering particle scanner as exemplified in the figure 5 below.

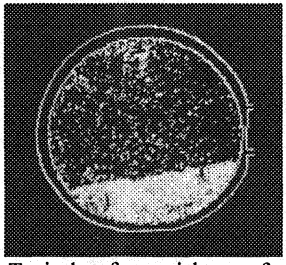

Figure 5. Typical wafer particle scan for Group B

A more detailed analysis using the AFM reveals "ring-like" residues shown in the micrograph.

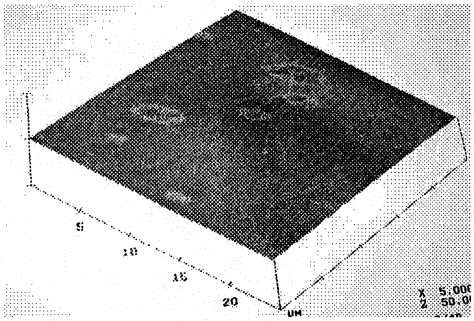

Figure 6. AFM micrograph of Group B residue

All wafers from the other groups did not exhibit any distinctive patterns. The resiliency of surfactant remaining on the silicon surface may be related to its adsorption [4]. Interestingly, there is no discernable pattern after oxidation and as mentioned earlier, the particulate levels on the wafer decrease. It may be speculated that the surfactant may volatilize during the thermal ramping prior to oxidation or the residues are masked by the oxide.

Based on the studies above, if metallic impurities exist in the dilute HF solution and the surfactant is not readily desorbed after rinsing, residues containing metallic impurities remain on the silicon surface. The residues may volatilize, be absorbed the growing oxide layer, and/or dissolve into the silicon crystal [10-12].

CONCLUSION

Addition of surfactants to dilute HF have been studied and shown to affect trace metals, particles, oxide thickness and minority carrier lifetime after a wet clean and thermal oxidation. Studies indicate that surfactants that potentially leave behind residues after the clean process can potentially lead to oxide thickness variations, higher metallic contamination, and degraded minority carrier lifetime.

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IMPROVEMENT OF SC-1 BATH STABILITY BY COMPLEXING AGENTS

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The effect of six different complexing agents, HEDP, TEA, EDTA, CDTA, DTPA and DTPMP, on the hot SC-1 bath stability was studied. Decomposition of hydrogen peroxide in the baths was monitored *in situ* by optical analyzer. The baths were intentionally contaminated with multimetal standard solution. Adsorption of metals onto wafers was studied using TXRF and GFAAS combined with VPD sample preparation. HEDP, CDTA and DTPMP were found to increase the bath lifetime as well as to decrease the adsorption of metals onto wafers.

INTRODUCTION

One of the major drawbacks of the SC-1 type (NH_3-H_2O_2-H_2O) silicon wafer cleaning solution is the continuous need of refreshment of the solution. The temperature of the cleaning solution is usually between 60 – 80 °C where NH_3 and H_2O evaporate as H_2O_2 decomposes according to Eq. [1]:

$$2H_2O_2\,(aq) \leftrightarrow O_2\,(g) + 2H_2O \qquad [1]$$

The evaporation may be suppressed to a large extent by using proper covers, whereas the decomposition is mainly caused by trace metal contamination, especially by Fe^{3+} and Cu^{2+}.(1) The metal contamination originates primarily from the chemicals, and therefore the continuous refreshment of the bath even accelerates the decomposition of hydrogen peroxide. As H_2O_2 normally constitutes the largest expense of the bath, its stability has significant economic value.

The decomposition of H_2O_2 can be prohibited by complexing the metals in the solution.(2) The complexing prevents the metals from reversibly changing their oxidation state. For example change between Fe^{3+} and Fe^{2+} causes the catalytic decomposition of H_2O_2 according to reactions [2] and [3].

$$2Fe^{3+}(aq) + H_2O_2 + 2OH^- \leftrightarrow 2Fe^{2+}(aq) + O_2\,(g) + 2H_2O \qquad [2]$$

$$2Fe^{2+}(aq) + H_2O_2 \leftrightarrow 2Fe^{3+}(aq) + 2\,OH^- \qquad [3]$$

The net reaction for [2] and [3] is [1]. Another benefit of the complexing agents is that the formation of soluble metal complexes also decreases the adsorption of metals to

wafer surfaces.(2,3) Without complexing agents metals often form complexes with OH^- ion in an alkaline solution. Especially neutral OH^- complexes such as $Fe(OH)_3$ and $Al(OH)_3$ are slightly soluble (4) and tend to deposit onto the wafers. Some metals form complexes also with NH_3 in the SC-1 bath, but those complexes are soluble and are not likely to adsorb on the wafers.

In the present study the stability of SC-1 solution was investigated by adding different complexing agents and simultaneously monitoring H_2O_2 lifetime in the bath by an infra red analyzer. The adsorption of metals was also studied by immersing wafers into solutions. In our previous paper (5) the adsorption was analyzed by spinning SC-1 solutions which contained metals and complexing agents on wafers.

The complexing agents which were tested are easily commercially available: hydroxyethylene diphosphonic acid (HEDP), ethylenediaminetetraacetic acid (EDTA), 1,2-cyclohexanediaminotetraacetic acid (CDTA), diethylenetriaminopentaacetic acid (DTPA) triethanolamine (TEA), and diethylenetriaminepenta methylenephosphonic acid (DTPMP). EDTA and DTPMP have been studied earlier (2) as well as for CDTA some data exists (6). All these complexing agents are known to form stable, soluble complexes with metals, especially with Fe^{3+}. Logarithmic values of room temperature stability constants are presented in the Table I. Constants of EDTA, CDTA, DTPA and TEA are from (4) and HEDP are from both (7) and (8). DTPMP constants are from (7), and the constant of Fe^{3+}-DTPMP –complex is from ref. (9). Two values for HEDP are shown because of contradictions in the data. Though the stability constants of TEA are rather low it was tested since it is a widely used complexing agent and in the literature it was stated that it might prevent Fe^{3+} from forming OH^- complexes.(10) Also in our previous studies TEA diminished the adsorption of iron.(5)

Table I Logarithmic values of stability constants (β values) of different complexing agents at room temperature.

	EDTA	CDTA	DTPA	TEA	DTPMP	HEDP
Ca^{2+}	10.7	13.1	10.8	0.8	6.7	6.8 (7) / 6.5 (8)
Cr^{3+}	13.6	23.0	-	-	-	-
Mn^{2+}	13.9	17.5	15.2	-	-	9.2 (8)
Co^{2+}	16.5	19.7	18.8	-	17.3	17.3 (7) / 9.4 (8)
Zn^{2+}	16.5	19.3	18.2	2.1	19.1	16.7 (7) / 10.7 (8)
Ni^{2+}	18.4	20.2	20.1	2.8	19.0	15.8 (7) / 9.2 (8)
Cu^{2+}	18.8	22.0	21.2	4.1	19.5	18.7 (7) / 12.5 (8)
Fe^{3+}	25.1	30.0	28.0	-	27.3	16.2 (8)
Al^{3+}	16.4	19.5	18.6	-	-	15.3 (8)

EXPERIMENTAL

The SC-1 cleaning solution consisted of 25 % NH_3 (VLSI, Merck), 31 % H_2O_2 (VLSI, Merck) and DI water. The ratio NH_3:H_2O_2:H_2O was 1:1:5. Adsorption of Al was tested also with a 1:10:50 solution. The volume of the bath was 30 l and the final temperature 65 °C.

The complexing agents were: HEDP (Wilson & Albright), TEA (p.a., Merck), EDTA (≥ 99 %, Fluka), CDTA (p.a., Fluka), DTPA (≥ 99 %, Fluka) and DTPMP (Solutia). The concentrations were 1 - 100 ppm. In the bath stability tests, metals were added from multielement (Cu, Fe, Ni, Mn, Ti, Zn) standard (J.T.Baker). The effect of Al, Fe, Mn and Cu was also studied separately with single element standards (J.T.Baker). The final concentration of each metal in the bath was 10 ppb. Al was tested also with 1 ppb. The deliberate contamination of the baths was essential in order to detect differences between chemicals more clearly.

A Horiba CS220 optical near infra red analyzer was used for the simultaneous and continuous monitoring of the concentrations of hydrogen peroxide and ammonia in the SC-1 cleaning baths. Metal adsorption studies were carried out by immersing wafers into the solutions for 10 minutes. Wafers were rinsed with DI water and dried with spindryer. The analysis of the metals heavier than z = 14 was carried out using Total Reflection X-ray Fluorescence Spectroscope (TXRF) (Atomika, TXRF8030W), equipped with tungsten X-ray tube and SiLi-detector. Aluminum was measured with Graphite Furnace Atomic Absorption Spectrophotometer (GFAAS) (PerkinElmer, AAnalyst600). The sample preparation was performed using Vapor Phase Decomposition (VPD) droplet collection system (GeMeTec, PADScan). In a VPD system, native SiO_2 layer is decomposed and the wafer is made hydrophobic by HF vapor in a polyvinyldifluoride chamber with open HF containers.(11) The sample is then collected from the wafer surface by automatically scanning a 50 µl droplet of either HF and H_2O_2 for TXRF analysis, over the wafer, or using a dilute HNO_3 droplet for GFAAS analysis. For TXRF the droplet is dried on the wafer whereas GFAAS samples are collected to vials and diluted to 200 – 2000 µl.

Residues of CDTA and DTPMP on the wafers were measured in separate experiments by Secondary Ion Mass Spectrometry (SIMS) with Ga^+ ions in the static mode. The samples were taken from the wet bench where about 400-700 wafers were cleaned during 3-4 hours. Samples were taken in the beginning and in the end of the period and the cleaning time was 8 minutes. 10 ppm of complexing agents was added only in the beginning, whereas NH_3 and H_2O_2 were added also during the cleaning period.

RESULTS AND DISCUSSION

Bath stability

Figure 1 shows the changes in the hydrogen peroxide concentration as 10 ppm (c(HEDP) was 100 ppm) of different complexing agents were added to the SC-1 bath. The bath was contaminated with the 10 ppb multimetal standard.

Warming up of the bath took about 50 minutes but the measurements were started from the cold solution. Without any complexing agents H_2O_2 decomposed about in an hour (curve labeled as "Metal"). For comparison, in uncontaminated bath 50 % decrease in hydrogen peroxide concentration took over 4½ hours. CDTA, DTPMP and HEDP stabilize the bath. With CDTA the concentration of H_2O_2 has decreased very slightly in three hours. The measurement was stopped after that. HEDP and DTPMP had a less complete effect. When copper was studied separately it was found that even 30 ppm of DTPMP does not fully stabilize solution which contains copper.

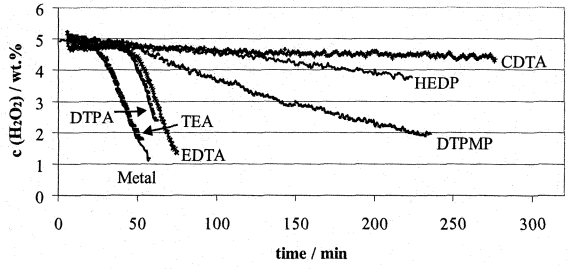

Figure 1. Change of the H_2O_2 concentration after the addition of complexing agents to the SC-1 bath.

Although in our previous spinning experiments TEA seemed to complex Fe^{3+} (5), in this study, as the temperature was raised to 65 °C, it did not work at all and hydrogen peroxide decomposed as fast as without any complexing agents. EDTA and DTPA inhibited the decomposition for 50 minutes but as soon as the bath was warm the concentration of H_2O_2 started to collapse. Therefore EDTA and DTPA were studied further by adding them also in the middle of the measurement (Fig. 2). After the addition of fresh complexing agent, H_2O_2 concentration stabilized for a while but started to decrease soon again. The temperature remained constant during the experiment.

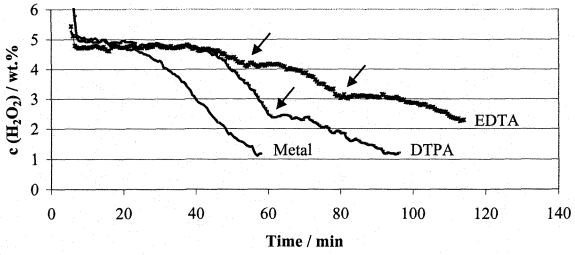

Figure 2. Change of H_2O_2 concentration when 10 ppm EDTA and DTPA were added during the measurement to the SC-1 bath. Additions are marked by arrows.

In our previous spinning experiments at room temperature it was found that pH of the SC-1 solutions with EDTA, DTPA and TEA increased in the process of time. On the other hand pH in SC-1 solutions with CDTA and DTPMP remained constant at least for 24 hours. It is concluded that EDTA and DTPA decompose in hot bath. Decomposition of EDTA has been mentioned also in Ref. (2). Although according to our previous experiments (5) TEA, EDTA and DTPA decreased the adsorption of metals onto the wafers they can not be used in the SC-1 baths due to their fast decomposition.

When the effects of iron, copper, and manganese were studied separately without complexing agents (Figure 3), it was seen that Fe^{3+} is almost alone responsible for the H_2O_2 decomposition and Cu^{2+} takes part to a lesser extent, as expected.(1) Manganese did not affect on the H_2O_2 concentration under the present conditions. H_2O_2 decomposition curve which is caused by copper correlates well with DTPMP curve in Figure 1.

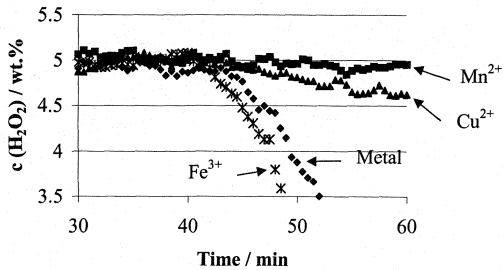

Figure 3. Effect of different metals on H_2O_2 concentration in the SC-1 bath. "Metal" denotes multimetal (Cu, Fe, Ni, Mn, Ti, Zn) standard + Al standard.

Adsorption of metals

The adsorption of metals was studied by immersing wafers into the stability test baths. Only the complexing agents which increased the bath stability, i.e. CDTA, DTPMP and HEDP were studied. Wafers were added as soon as the bath was hot i.e. about 50 minutes after the solution preparation.

The surface concentrations of adsorbed metals in SC-1 which contained 10 ppb multimetal standard without complexing agents are shown in Table II. The amounts of adsorbed metals are similar to earlier experiments where Al, Cu, Ca and Fe were studied.(12)

Table II Surface concentration of metals adsorbed from SC-1 contaminated with 10 ppb metal standard.

	Fe	Cu	Mn	Ni	Zn	Ca	Al
c (x 10^{10} at./cm^2)	150-770	0.4-2.0	0.2-0.7	5.0-8.5	73-123	11-19	1500-2000

Table III represents the effects of the complexing agents on the metal residue on the wafers compared to the uncomplexed bath. 100 at.% residue means that the same amount of metal was analyzed from the wafer in the presence of complexing agent as without it. The residues are rather expected on the basis of stability constants (Table I) and they are congruent with our spinning experiments (5). Manganese residues seem to be rather large but those values are a bit uncertain since the total amount of adsorbed Mn is small (c.f. Table II). Adsorption of Ca and Al is difficult to diminish. Especially for Al the total adsorbed amount is large.

Table III Metal residue on the wafers.

Complexing agent in the bath	concentration (x 10^{-6} mol/l)	Fe at.%	Cu at.%	Mn at.%	Ni at.%	Zn at.%	Ca at.%	Al at.%
CDTA 10 ppm	29	4	<0.9	50	2	0.2	20	34
DTPMP 10 ppm	8.7	0.1	430	20	2	110	30	26
HEDP 100 ppm	243	0.1	3	20	2	0.2	45	51

The amount of adsorbed copper is larger in the presence of DTPMP than without it if Cu was added using multielement standard. Similar behavior was not observed when it was added using single element standard. The same has been observed also in Ref. (2)

Fe and Cu, which effect on the bath stability, and Al, which adsorbs the most efficiently, were studied also separately using single element standards. The adsorbed metal concentrations were measured from the wafers in stable baths. In all cases the concentration of iron or copper was 10 ppb which is about 0.2 μmol/l. For iron 1.6 ppm (1.4 μmol/l) of DTPMP, 5 ppm (14.5 μmol/l) of CDTA or 30 ppm (72.8 μmol/l) of

HEDP was enough to prevent H_2O_2 decomposition and decrease the metal residue on the wafer to below 0.5 % of the original level. In the case of copper 2.4 ppm (6.9 µmol/l) of CDTA was enough to prevent H_2O_2 decomposition and decrease the metal residue on the wafer below the detection limit of TXRF. 100 ppm (243 µmol/l) HEDP decreased the adsorption to 3 at. %. 30 ppm (26.2 µmol/l) DTPMP decreased the residue only to 50 at.%. Cu-DTPMP-bath was not stable either.

The adsorption of aluminum was found to be the most difficult to prevent. When the temperature was lowered from 65 to 30-50 °C or the metal concentration was decreased from 10 to 1 ppb the total amount of adsorbed Al decreased but the residue with the complexing agent remained always above 20 at.%. The increase of the complexing agent concentration from 10 to 100 ppm did not decrease the residue either. But when SC-1 was diluted and pH of the solution was lowered from about 11 (NH_3:H_2O_2:H_2O = 1:1:5) to about 10 (NH_3:H_2O_2:H_2O = 1:10:50) the residue diminished to below 3 at.% in 10 ppm DTPMP bath. This behavior can be explained on the basis of aluminum hydroxide (4) and Al-DTPMP stability constants. The Al-DTPMP complex is more stable at lower pH.

Residues on the wafers

The analysis of complexing agent residues on the wafers has been started from baths which contains CDTA or DTPMP. In preliminary studies no organic contamination was detected from wafers in the DTPMP bath neither at the beginning nor at the end of the cleaning period. On the other hand small amounts of organic contamination were found from some wafers in the CDTA bath at the end of the cleaning period. The residue could not be identified as being from CDTA and the samples were very unlike, i.e. the result was not reproducible. SIMS studies will continue and, in addition, the residue will be studied by capillary electrophoresis. For comparison, in Ref. (2) DTPMP residues were not detected on wafers either.

CONCLUSIONS

The use of complexing agents is a very promising method to improve the SC-1 bath lifetime and decrease the chemical costs. In the present study the effect of complexing agents on the SC-1 bath stability and adsorption of metals were tested with six different chemicals. CDTA, DTPMP and HEDP prohibited the decomposition of hydrogen peroxide and increased the bath stability effectively. In addition they decreased the adsorption of metals onto the wafers if relatively large excess of complexing agent was used. Adsorption of Al may be prevented by DTPMP by using more diluted solution than the conventional 1:1:5 SC-1. In order to achieve true savings in chemical costs the stability of metal complexes in hot, alkaline and oxidative SC-1 baths is a very important issue. Therefore our further studies will be focused on stability tests of complexing agents. In addition chemical residues need to be studied carefully.

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PREVENTION OF Si ETCHING IN DILUTED SC1 SOLUTIONS

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Very diluted SC1 solutions at low concentrations (1:1:50 or more) are used to maintain a reasonable chemical consumption in single tank or single wafer tools. In these conditions, SC1 behaviour is different from conventional high concentration chemistries used in re-circulated systems, and severe defectivity and electrical issues may arise due to silicon etching. In this paper we show that it is possible to overcome this problem by a strong oxidising step before SC1, performed injecting ozonised water. This step grows a relatively thick and robust chemical oxide that prevents direct silicon etching by OH- ions, reducing the amount of etched silicon, without compromising the electrical characteristics and the particle removal efficiency.

INTRODUCTION

In wet cleaning process, SC-1 is commonly used in the semiconductor industry to remove light organics and particles. During this step, the silicon is oxidised and dissolved at the same time. In order to reduce the cross-contamination risk from one lot to the next one and to simplify the hardware configuration of last generation single tank and single wafer processors, several equipment manufacturers propose to use a "one-shot", always fresh chemicals. In order to ensure an acceptable chemical consumption, it is therefore necessary to use very diluted solutions, such as: 1:1:50, 1:3.3:80, 1:2:50, 1:1:>200... These conditions become very different from the re-circulated chemistries used on conventional wet benches, where DIW/ammonia ratio is usually 10~20 and peroxide/ammonia ratio 2~4.

In a previous study[1], the evaluation of a diluted SC-1 in an industrial environment was presented, both on full sheet wafers -i.e. particle removal, roughness and silicon consumption- and on real MOS structures. Several pitting and electrical issues were found, when using diluted SC1, especially for low peroxide/ammonia ratios or high temperatures and when SC1 was preceded by a HF step. A strong correlation was also confirmed (Figure 1) between the amount of etched silicon and the number of COPs (Crystal Originated "Particles"), revealed as particles by particle measurement tools based on light scattering[2]. Particle addition is also very sensitive to the substrate quality, and it is anyway much less if EPI substrates are used.

K. Yamamoto et al. explained this phenomenon[3] claiming a kinetic reaction model of Si substrate with APM, where the etching reaction of Si substrate proceeds along two paths (path-1 and path-2). In path-1, the silicon surface is oxidised by HO_2^- and then the SiO_2 layer is etched by OH^-. In path-2, OH^- directly etches the Si surface. We can hence assume that path-2 reactions occur when the oxide grown by HO_2^- ions is thin or weak enough to allow the diffusion of OH- ions. This happens in case of low H_2O_2 concentration mixtures, such as diluted APM solutions. Path-2 reaction has a much higher Si etch rate than the oxidation-etching reaction, and according to reference 2, it generates a higher amount of defects.

It was also observed[1] that the number of defects is much higher when SC1 is preceded by an HF step. Figure 2 reports the number of defects at 0.12μm, as a function of the number of cleanings for a diluted SC1, with and without a preceding HF, and for a conventional recirculated 1:4:20 SC1, with the same process temperature and time. A high concentration SC1 has a very low particle addition with respect to a diluted one and the HF step clearly enhances the defect growth rate. These defectivity data are correlated with the amount of silicon etched, as shown in Figure 1.

In this paper, we will study the differences between SC1 and HF-SC1 treatments, and we will propose a way to overcome the excessive silicon etching that is the cause of the severe defectivity problems mentioned above.

EXPERIMENTAL

Etching of silicon surface is a very challenging measurement, because it cannot be carried out using the conventional optical methods, without SOI substrates. Anyway, a good approximation[1] can be obtained using amorphous silicon (α-Si) on an oxidised substrate and measuring the α-Si thickness by Spectroscopic Ellipsometry (SE), by the three-layer model illustrated in Figure 3. SE can provide the thickness of the bottom oxide layer, of the α-Si and of the top oxide layer as well as information on α-Si/poly-Si crystalline degree. Repeatability of the measurement of the α-Si layer is usually of the order of 0.1Å. The thickness of the three layers was measured on 13 points per wafer. Therefore, SE technique provides a direct measurement of the amount of Si etched.

A Design of Experiment (DOE) was performed to evaluate the amount of silicon etched as a function of chemical concentration, bath temperature and dip time, for both SC1 and HF-SC1. A short recipe description is reported in Table 1. Experiments were executed on a DNS FC821L wet station, using an ONB tank. In this tool –as well as in other single tank tools–, chemicals are injected into the bath, than wafers are dipped in a static solution and rinsed *in-situ*. During the dip, the temperature of the bath slightly decreases, because the quartz tank is not heated. In all the experiments SC1 chemical ratio was kept constant at 1:2:100 (NH_4OH:H_2O_2:H_2O). dHF concentration was 0.3%-wt.

Step	SC1	HF-SC1
1		0.3% dHF injection
2		dHF dip (180")
3		OFR
4	Hot DIW	Hot DIW
5	1:2:100 SC1 injection	1:2:100 SC1 injection
6	SC1 dip with megasonics	SC1 dip with megasonics
7	QDR/OFR	QDR/OFR
8	Drying	Drying

Table 1: SC1 (left) and HF-SC1 (right) sequences

RESULTS AND DISCUSSION

Figure 4 shows the amount of α-Si etched at 60°C as a function of dipping time for SC1 and HF-SC1 treatments. The "0" value on the *x*-axis refers to the end of the chemical injection and the beginning of the dip time (step 6 in Table 1). After chemical injection about 13Å of α-Si are already removed by HF-SC1 treatment, while only a few Å are removed by SC1 without any preceding HF step.

To explain the different etching and defectivity behaviours of HF-SC1 and SC1 only treatments, it can be supposed that after an HF treatment, silicon is hydrogen passivated and it is exposed to APM without any protecting native oxide (Figure 5). Therefore, at the beginning of the APM process, there is a relatively short time (hereafter referred as t_i) when silicon is exposed directly to OH^- ions before being oxidised. In these conditions ($t<t_i$), path-2 reaction prevails, because there is no oxide –or at least a very weak and porous chemical oxide- acting as a barrier for the OH^- diffusion towards the silicon surface. After this phase ($t>t_i$), silicon is oxidised by HO_2^- ions, and path-2 reaction becomes less important while path-1 reaction becomes dominant. In these conditions, there is a stable oxidation-etching reaction, only determined by temperature and chemical concentration and the behaviour turns out to be the same of an SC1 treatment without any preceding HF step. This explains why SC1 and HF-SC1 curves are parallel – same etching rate- in Figure 4. Because the silicon oxidation rate by HO_2^- ions is very fast even at low temperature[4], it can be supposed that t_i is very short at usual process temperature, of the order of few seconds at 50°C.

In order to avoid path-2 reactions during the initial phase it is necessary to protect silicon against OH- direct etch by creating a protective chemical oxide. The first attempt was carried on using 1:50 hydrogen peroxide injection for 300" at both room temperature and 50°C. Anyway, as shown in Figure 6, the insertion of a peroxide pre-injection step does not provide any benefit. Indeed, as reported in reference 5, in case of H_2O_2 oxidation the surface is not completely oxide covered even after a long exposure period. By *in-situ* infrared spectroscopy, it was demonstrated that oxide on a HF treated surface growth is

compatible with an "island like" model, and Si-H_2 bonds are present even after several minutes of exposure to 3% H_2O_2. In our experiments, we used more diluted (0.6%) peroxide than the one in reference 5, and when the surface is exposed to APM it is still mostly hydrogen passivated and hence path-2 direct etch mechanism takes place. Oxide thickness grown by 50°C, 1:50 H_2O_2: H_2O is reported in Figure 7.

In the same paper (ref. 5), it is also reported that just 2ppm of ozonated water produce a much faster surface coverage and that Si-H_2 bonds disappear after about 5', and the surface becomes completely covered by chemical oxide in a relatively short time. In our test, the ozone was generated by a membrane type diffuser, with a concentration of 15ppm in 20l/min water flow. In these conditions, a high quality chemical oxide grows in a very short time. A similar approach was also used in reference 6 to reduce silicon etching for SOI substrates.

Thickness as a function of DIW/O_3 injection time was measured by SE on bare silicon wafers and it is reported in Figure 7. In the same chart, it is also plotted the thickness grown by peroxide at 50°C.

Oxide grows very quickly in ozonised DIW and a relatively thick oxide can be obtained in about 50-100", while in diluted peroxide, oxide thickness is much lower, even at 50°C and after 300" injection.

When a recipe has to be implemented on single tank or single wafer tools, process time is inversely proportional to the equipment throughput; therefore, the passivation and subsequent rinse steps must be as short as possible. This can be easily achieved using ozonised DIW. In fact, as shown in Figure 8, about 60" of DIW/O_3 injection are already enough to reduce Si etch. In this figure, the amount of α-Si etched during an HF-DIW/O_3-SC1 treatment is reported as a function of DIW/O_3 injection time, at SC1 temperature of 50°C and 60°C. In the same chart it is also reported the amount of α-Si that is oxidised by DIW/O_3 (about 4-5Å).

In case of SC1 at 50°C for 300", any etching by the SC1 itself is almost completely avoided. In fact, the amount of α-Si etched (~6Å) is very close to the one consumed by the Si oxidation mechanism of DIW/O_3. In case of a standard HF-SC1 process, without any intermediate DIW/O_3 injection, about 20Å of α-Si are etched. When SC1 is performed at higher temperatures, such as 60°C, the chemical oxide grown by DIW/O_3 is completely removed and silicon starts to be etched by SC1. In Figure 9 is reported the amount of α-Si etched by HF-DIW/O_3-SC1 treatment, with DIW/O_3 injection time of 300", as a function of SC1 temperature. SC1 dip time has been kept constant to 300". Dashed line shows the amount of Si consumed by the DIW/O_3 oxidation itself. If a low silicon etching is required, APM temperature should not be more than 50°C.

Another confirmation of the capability of the DIW/O_3 treatment to reduce silicon etching has been obtained substituting the SC1 step with diluted ammonia (dNH_4OH). In this way, we could exclude any influence of H_2O_2 and focus only on the quality of the DIW/O_3 oxide. In Figure 10 is reported the amount of α-Si etched by 0.03% NH_4OH at 50°C preceded by a HF step, with and without an ozonised water passivation treatment. In these process conditions ammonia can remove about 400Å, which means an etch rate of 1.1Å/s. Such a high etch rate can explain why t_i is so small. In case of the HF-DIW/O_3-

dNH_4OH process, the amount of etched α-Si is reduced to about 200Å; this means that pure ammonia takes about 3 minutes to remove the chemical oxide grown in the ozonised DIW. The effect of the ozone pre-injection step on the LPD addition is reported in Figure 11. The experiments were carried out using CZ wafers and SC1 temperature of 50°C and 60°C, with and without a DIW/O_3 intermediate-injection step. In the chart, it is reported the number of LPDs measured after three sequential cleaning treatments.

The HF-SC1 treatment at 60°C is much more critical than the 50°C one. DIW/O_3 injection step, allows a significant reduction of the amount of added defects, and at 50°C there is almost no increase in LPD counts after the cleaning sequence. In Figure 12, the treatments with diluted SC1 are compared with a HF-SC1 standard sequence at higher SC1 concentrations, but with the same temperature (50°C) and process time (300").

When the HF-SC1 sequence is performed using a concentrated SC1 solution, the amount of etched silicon is considerably less then the one etched by the same sequence, using a diluted APM mixture. HF-DIW/O_3-SC1 allows a further reduction of silicon etching to the level of an APM step itself.

CONCLUSIONS

The excessive amount of etched silicon by diluted SC1 (and the consequent generation of silicon defects) very often causes electrical and defectivity problems when preceded by a HF step. In order to overcome this problem, diluted SC1 is sometimes used at relatively low temperature, but this have a detrimental effect on particle removal efficiency. In this paper, we have summarised the Si etching mechanism in SC1 and introduced a way to avoid, or at least to reduce this problem by inserting a DIW/O_3 injection step in the standard HF-SC1 sequence. The shielding capability along with the perfect cleaning efficiency of the ozonated water was proven and compared with H_2O_2.

Moreover, due to the short time required by the DIW/O_3 step, there is not any meaningful increase in the cleaning cycle time.

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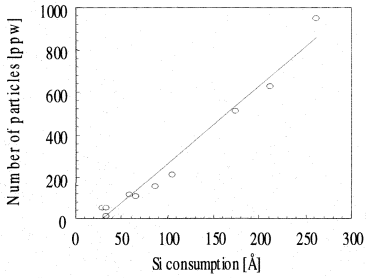

Figure 1: LPD number @0.12µm as a function of silicon etching

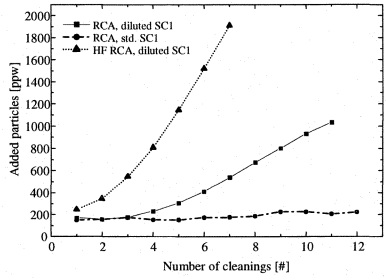

Figure 2: LPD addition @0.12µm as a function of the number of cleanings

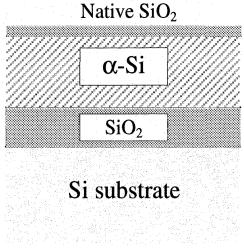

Figure 3: Model used for SE measurements.

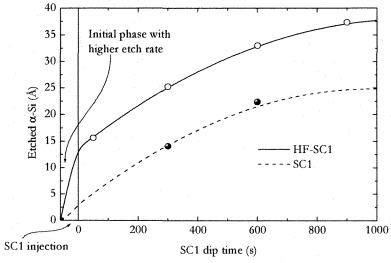

Figure 4: Etched α-Si for 1:2:100 SC1 at 60°C and HF-SC1.

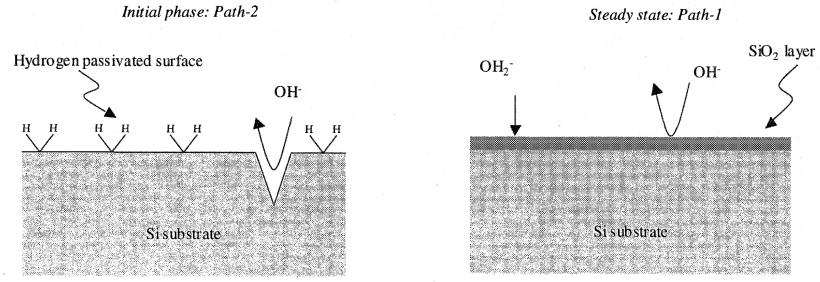

Figure 5: Reaction paths for $t<t_i$, (left) and for $t>t_i$ i (right)

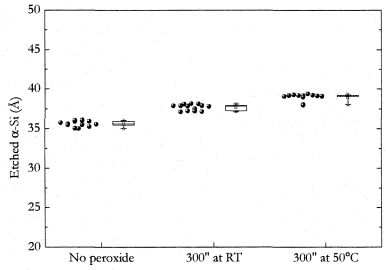

Figure 6: Etched α-Si for 1:2:100 SC1 at 60°C as a function of peroxide pre-injection in the sequence HF-H_2O_2-SC1.

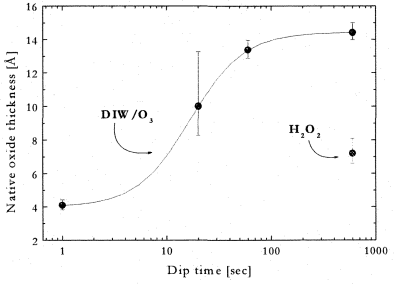

Figure 7: Oxide growth by 15ppm DIW/O_3 and H_2O: H_2O_2 (1:50, 50°C).

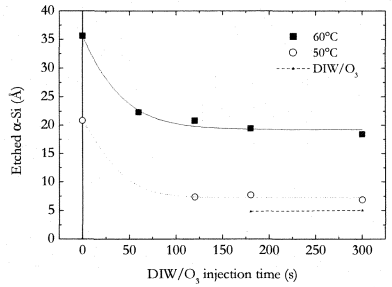

Figure 8: α-Si etching by HF-DIW/O_3-SC1 Vs DIW/O_3 injection time.

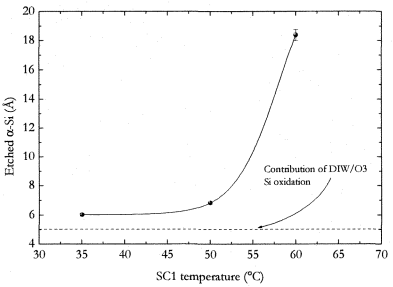

Figure 9: α-Si etching by HF-DIW/O_3-SC1 as a function of SC1 temperature.

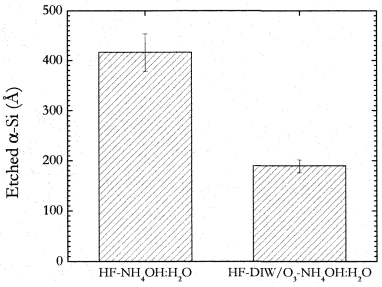

Figure 10: α-Si etching by HF-NH_4OH:H_2O and HF-DIW/O_3-NH_4OH:H_2O. T=50°C, NH_4OH:H_2O ratio 1:50.

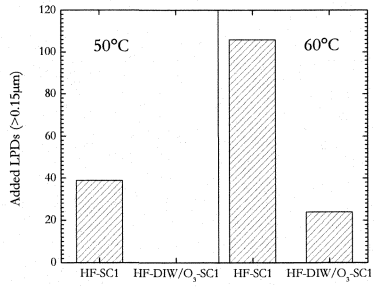

Figure 11: Average LPD addition at 50°C and 60°C HF-SC1 processes.

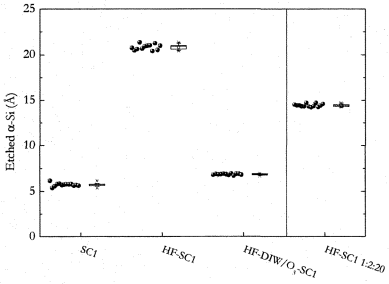

Figure 12: α-Si etching by 1:2:100 SC1, HF-SC1 and HF-DIW/O_3-SC1 at 50°C, compared to HF-SC1 (1:2:20).

INSITU PRE-EPI CLEAN PROCESS FOR NEXT GENERATON DEVICES

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Advanced ULSI devices require replacement of current high temperature dry cleaning steps, that are used to remove the native oxide, with lower temperature processes. As a result, prior wet-cleaning steps must yield the lowest defects possible on the wafer surface. In the present study, different pre-epitaxial cleaning processes are investigated. A conventional multi tank HF-last process is compared to a single step insitu HF-last process. Experiments showed that the use of dilute chemicals and insitu HF/Rinse/Drying yield better results than conventional multi-tank wafer processing.

INTRODUCTION

With further reduction of the dimensions of the microelectronic devices into the low nm scale, the cleaning procedures play an increasingly important role in IC manufacturing. The process chemicals, sequence and number of cleaning steps are becoming more critical in determining the desired end results [1,2]. High temperature (>1050° C) gas phase cleaning is typically used to dissolve the native oxide and any other contaminants on the wafer surface prior to epitaxial growth [3]. Advanced low temperature epitaxial processes for advanced ULSI devices require this high pre-epitaxial thermal budget be lowered considerably [3]. However, the lower the temperature the lower the desorption rate of SiO_2. To alleviate this problem, an HF-last process is typically used to produce an H-terminated surface. This process when done properly would yield a surface with the lowest defects [4] and therefore allow the pre-bake and desorption temperature to be substantially lower than 1050° C. In the present study, different pre-epitaxial cleaning processes were investigated. A conventional multi-tank HF-last process was compared to a single step insitu HF-last process. Results showed that dilute chemicals and insitu HF/Drying are key factors to successful wafer processing for IC manufacturing.

EXPERIMENTAL

Experiments were conducted on Akrion's GAMA-1™ automated wet station. The tool is capable of running two process sequences; multi-tank and single tank insitu process. Wafers were processed in the tool prior to the epitaxial growth steps. To simulate a patterned wafers situation, silicon wafers were sandwiched between the dummy oxide wafers. This provided the most challenging contamination levels to the silicon wafers from the oxide wafers since etch byproducts are deposited from the oxide wafers onto the bare silicon wafers. Different cleaning techniques were used to remove this high contamination level. The conventional sequence of SC1/Rinse/HF/Rinse/Dry was used

first to remove the contaminants. Surfactant was mixed with HF as part of the process development. A modified insitu cleaning sequence was developed for minimum particle deposition. Details of experimental procedure and materials used are shown in Tables 1 and 2.

RESULTS AND DISCUSSION

In order to reduce the thermal budget for Si epitaxial growth, the surface conditioning step has been shown to be critical. Typically, a high temperature H_2 prebake is used to desorb the native oxide and to prepare an ideal surface for epitaxial layer deposition. However, for advanced next generation devices, temperatures as low as 700° C are required [5,6] to ensure isothermal processing.

Tests were conducted to ensure the process steps and equipment are particle neutral. Even in the presence of the oxide wafer fillers, particle addition was kept at an absolute minimum. As shown in figure 1, the average particle addition is – 6 (1 σ = 11). When using only bare silicon wafers, the conventional HF-last process yields low particle addition, as shown in figure 2. The average particle addition was less than 40 particles at 0.12 μm. In addition, post-epi defects were also fairly low (~ 1.26 defects/cm^2), as shown in Figure 3.

In IC manufacturing wafers are typically mixed with oxide wafers or the wafers are patterned. Typically, exposed silicon is adjacent to oxide or nitride areas. In HF solutions, etch byproducts will be transported from the hydrophilic surface to hydrophobic surfaces. This results in high particles counts on the exposed silicon. The process has to be designed to overcome these issues. As explained in the experimental section, silicon wavers were sandwiched between oxide fillers to simulate typical wafer manufacturing.. Results show that conventional HF-last process used in this situation (SC1/Rinse/HF/Rinse/Dry) produces high particle counts at 0.12 μm (>10,000) as shown in figure 4. Consequently, the post epitaxial defects were also high (>30 000, not shown). These LPDs (light point defects) are considered to be nucleation sites during the epitaxial deposition. Conventional wafer transfer between tanks plays a significant role in increasing silicate deposition into silicon wafers.

Two approaches were taken to prevent particle deposition during the etch process. In the first method, surfactant was added to the HF bath as a way to improve the wettability of wafers and hence reduce particle deposition onto the wafers. Better process results were obtained when compared to conventional process. However, the presence of any trace amounts of the surfactant remained problematic in the epitaxial growth process. Additional chemistries would have to be added, e.g. ozone, to remove any trace amounts of the surfactants. A second process needed to be developed; one that eliminates the need to use surfactant. The approach taken was to minimize exposing the wafer to an air/liquid interface where contaminants may reside. These contaminants will deposit on the wafers

during insertion into or pulling out of the liquid. A chemical injection scheme was used to process the wafers in the dryer. When wafers were processed with no transfer between cleaning steps, much lower particle deposition was obtained. As shown in figures 5 and 6, an average of less than 50 particles were added to the wafers. It is important to mention here that the use of ozonated rinse after HF and before going to the SC1 step is very critical in eliminating any potential for metal-induced pitting on the hydrophobic surface [7]. As reported by Knotter [7], Fe for example in the SC1 can induce pitting on hydrophobic surface. The oxide chemically grown in the ozonated rinse is stable and thick enough (7-10 A, see figure 7) to protect the silicon surface from any metal roughening effects. The post-epi cleaning results for the insitu method are shown in Figure 7. The average LPD density per wafer is about 0.89 defects/cm2. This level is significantly lower than any published data at 0.12 um. Clearly, the lower the HF-last defects the lower the post-epi deposition defects as shown in figure 8.

The results of different cleaning recipes are summarized in table 3. Different wafer types were used also as fillers to investigate if the filler wafer type has any negative impact on the results. The results showed that the most critical step to achieve extremely low post epi deposition defects is the insitu HF/Rinse/Dry with no wafer transfer between steps. Measurements were also taken to characterize the background oxide thickness as a measure of the [O] content on the wafer surface. Time constraints prevented the use of more sophisticated analytical techniques e.g. EDX, Auger, . . .etc. to characterize the [O] concentration in a timely fashion. It is equally important to notice that the amount of [O] present on the wafer surface could significantly increase the particles deposited on the wafer. The lower the [O] content on an H-passivated surface the lower the particle deposited as shown in figure 9.

CONCLUSIONS

A modified insitu cleaning procedure was developed for pre epitaxial growth. Results show significant improvement when compared to a conventional HF-last cleaning process. The insitu processing (one step etch/rinse/dry) has shown to be a key factor in eliminating particle deposition on exposed silicon areas on the wafer surface. Experiments showed that the use of dilute chemicals and insitu HF/Rinse/Drying yields significantly lower defects (post clean and epitaxial deposition) than those obtained during conventional multi-tank wafer processing.

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Table 1: Experimental Procedure

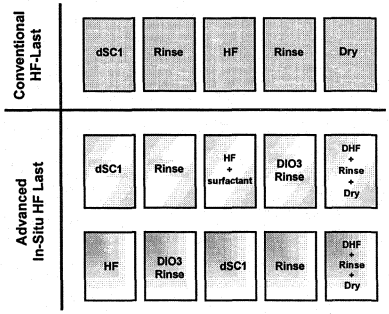

Table 2: Experimental Material

- Fully Automated GAMA (50x200 mm)
- LuCID dryer w/ HF controlled injection
- 3 mm EE (Omega composite carrier)
- KLA-Tencor Surfscan calibrated at 0.12 µm
- Low count Si wafers were placed between oxide dummy wafers
- HF ~ 100:1 @ ambient temp.
- DHF ~ 400:1 @ ambient temp.
- dSC1 ~ 1:2:50 @ 50 C and 800 W
- DIO3 rinse ~ 5 ppm at ambient temp.
- DO_2 was controlled < 1 ppb
- ASML Reactor

Table 3: Critical Step ⇒ In-Situ HF-Last in Dryer

Cleaning Recipe	48 Filler Wafs	LPD Sum @ > 0.12um			Rudolph post-cln oxide (A)	Rudolph post-cln 1 Sigma	Post-Epi LPD >0.12um
		Pre-Clean	Post-Clean	Delta			
SC1/OCR/HF(+surft)/OCR/LuCID(inj HF+R+Dry)	TOX	3	16	13	4.390	0.256	66
	TOX	15	27	12	4.275	0.188	379
	TOX	8	45	37	4.201	0.234	211
SC1/OCR/LuCID(HF+R+Dry)	TOX	9	73	64	4.728	0.414	329
	TOX	10	12	2	4.553	0.294	267
OCR/LuCID(HF+R+Dry)	TOX	4	30	26	4.805	0.133	377
	TOX	8	40	32	4.7	0.117	250
HF/OCR/SC1/OCR/LuCID(inj HF+R+Dry)	TOX	8	87	79	4.51	0.191	241
	TOX	3	57	54	4.459	0.107	125
	TOX	10	62	52	4.362	0.142	185
HF/OCR/SC1/OCR/LuCID(stg HF+R+Dry)	TOX	33	87	54	4.351	0.095	243
	TOX	28	16	-12	4.37	0.124	524
	poly & ntrd	5	16	11	4.389	0.095	227
	poly & ntrd	5	91	86	4.341	0.129	430
	poly & ntrd	6	20	14	4.334	0.112	158
	poly & ntrd	26	9	-17	4.288	0.087	141
	poly & ntrd	5	10	5	4.258	0.134	257
	TOX	3	29	26	4.584	0.18	242
	TOX	4	62	58	4.501	0.231	335
	TOX	2	12	10	4.252	0.113	207
	TOX	14	32	18	4.325	0.126	322

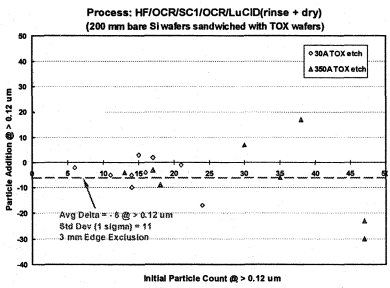

Figure 1: Particle Performance with Simulated Pattern Oxide Etch (Hydrophilic at End)

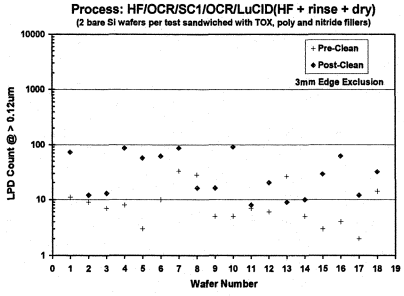

Figure 2: Conventional HF-Last without TOX Pattern in Presence (Bare Si Only)

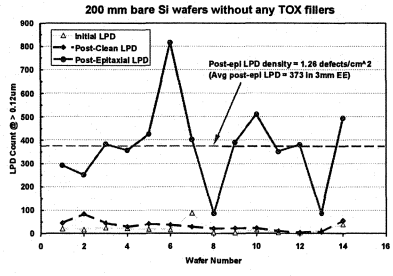

Figure 3: Post-Epitaxial (900C Bake) LDP after Conventional HF-Last Process

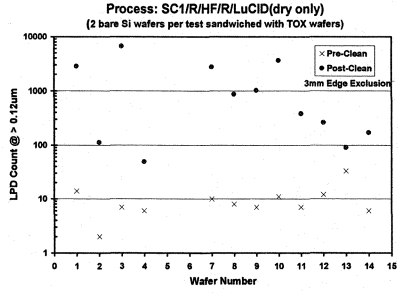

Figure 4: Conventional HF-Last with Simulated Pattern Oxide Etch (silicate contamination)

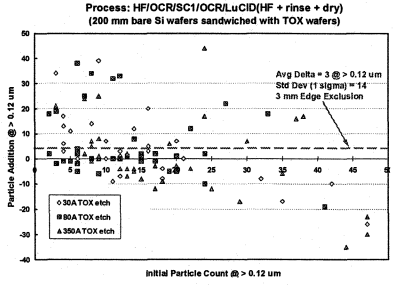

Figure 5: Particle Performance with Simulated Pattern Oxide Etch (Hydrophobic at End)

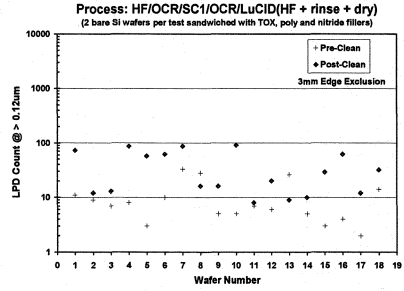

Figure 6: In-Situ HF-Last with Simulated Pattern Oxide Etch

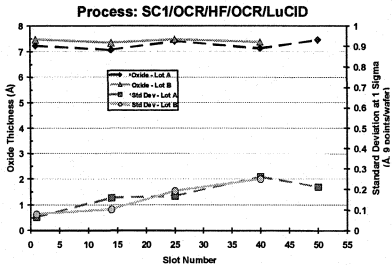

Figure 7: Oxide Regrowth Uniformity by OCR

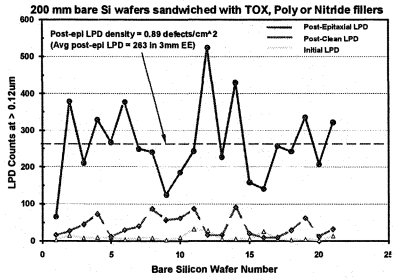

Figure 8: Post-Epitaxial (900C Bake) LDP after In-Situ HF-Last in the Dryer

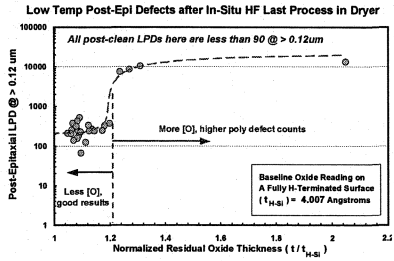

Figure 9: Low Silicate Particles and Low Residual Oxide Content on Surface are Crucial

ADVANCED PRE-GATES FOR HIGH QUALITY THIN OXIDES AND NITRIDED OXIDES

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In this paper we report on the effect of pre-gate cleaning techniques on the Gate-oxide Integrity (GOI) of thin oxides and nitrided oxides. Test wafers were prepared to compare the GOI of several pre-gate wet immersion cleaning techniques for 40-65Å thin oxides and nitrided oxides. The cleaning efficacy was evaluated by characterizing particle contamination levels, surface roughness, charge to breakdown, and oxide thickness. The effect of particles, micro-surface roughness, and metallic contamination on GOI was also revisited. Dilute RCA pre-gate cleans demonstrated better electrical performance than conventional RCA and HF-last processes.

INTRODUCTION

Device scaling laws require thinning of the gate dielectric in a MOS transistor to maintain the device transconductance(1). With 180nm and 130nm devices currently in full production, gate oxide thicknesses of 40Å or less are routinely used. In these thickness ranges, it becomes difficult to produce a SiO_2 film with consistent and reliable operating characteristics.

Nitrided oxides, SiO_xN_y, with their higher dielectric constant, have been routinely used to decrease the equivalent oxide thickness, thereby increasing the transistor drive current (2, 3). In addition, it is proposed that the pile up of nitrogen at the Si/SiO_xN_y interface acts as a strain relief mechanism which reduces the density of interface traps, D_{IT}, and improves the oxide reliability (4).

While the effects of oxide growth conditions in furnaces have been thoroughly investigated, (5) the role of wafer surface preparation on thin oxide characteristics is not as well understood. The impact of high levels of particle contamination on film deposition and growth have long been known, (5, 6) and several studies have identified the role of specific metal ion contaminants on GOI (7, 8). This paper studies the impact

of wafer cleaning on both the electrically measured gate oxide integrity (GOI) and the physical characteristics of the Si surface. The effect of wet chemical immersion pre-gate cleans, were first investigated using conventional linear wet benches with stand-alone process and rinse tanks. These were then compared to SCP's new platforms that incorporate advanced cleaning processes with combined ultra-dilute process/rinse/dry steps in a single chamber. This type of system is highly desirable because it offers greater control over the environmental conditions in which the wafers are exposed to. In addition, it reduces the wet bench footprint and Cost of Ownership (CoO).

EXPERIMENTAL

Device Fabrication

P-type <100> wafers with an initial resistivity of 6-9 Ω-cm were processed using the sequence shown in Figure 1 to fabricate electrical GOI test devices. The advanced CMOS process flow incorporated a double retrograde well with a recessed field oxide. The gate oxidation process was performed in a vertical furnace. After the thermal oxidation process, the wafers were annealed at a higher temperature in an RTP under a nitrous oxide environment. After the RTP process, the wafers were further processed to define poly-Si gate electrodes and metal contacts for electrical probing.

Pre-Gate Cleans

The pre-gate cleans investigated in this study fall within three major categories.

1. Standard RCA cleans (9) using concentrated SC1 and SC2 chemistries;
2. Dilute RCA(dRCA) cleans using ultra dilute SC1 and SC2 chemistries ;
3. HF-last passivation cleans which result in a hydrogen-terminated surface state.

Ref. RCA (standard RCA clean): This pre-gate cleaning process is performed in a traditional linear wet bench that uses a spin dry technique at the end of the process sequence. This clean was included as a benchmark since it is currently used in a high yielding CMOS process line.

DRCA (dilute RCA): This pre-gate clean utilized a SCP linear wet bench with advanced processes that uses an IPA vapor displacement drying technique combined with a final rinse step in a single chamber (SCP GreenDry technology (GD) (10). This rinse/dry chamber also incorporated the option to inject dilute chemistries (CI) during the final rinse phase (GD-CI). This was used to inject dilute HCl prior to the final rinse/dry in the dRCA process. It was also used to inject O3 gas and dHF for final passivation steps prior to rinse/dry.

HF-last splits all involved HF-last cleans performed in a small footprint platform which included an HF recirculated process tank (used for sacrificial oxide strip) and a second tank with an integrated rinse/IPA vapor dry (GD), This rinse/dry chamber also incorporated the option to inject dilute chemistries (CI) during the final rinse phase for surface passivation/clean.

Prior to the pre-gate cleaning step, a HF etch to strip the 300Å sacrificial oxide was performed. After each of the pre-gate cleans, the staging time prior to oxide growth was carefully controlled to less than an hour.

Surface Characterization

Particle contamination levels before and after pre-gate cleans were monitored using a KLA-Tencor Surfscan SP1 at a threshold diameter of 0.12μm. Particle contamination levels were measured with a threshold diameter of 0.12μm.

Si surface roughness measurements following the pre-gate cleaning splits were performed using a Digital Instruments NanoScope5000 AFM.

Metallic contamination levels on bare Si wafers after the pre-gate clean splits were evaluated using VPD-ICP-MS. The metal species analyzed, (detection limit at 10^{10} atoms/cm^2), were Al(0.3), Ca(0.2), Cr(0.1), Cu(0.05), Fe(0.1), Mg(0.3), Ni(0.05), K(0.2), Na(0.2) and Zn(0.06). It should be noted that all the chemicals used in the study were ppb grade chemicals.

Ellipsometry was used to measure the thickness of the oxide after the furnace oxidation and RTP processes.

Electrical Characterization

Electrical GOI Testing: GOI was characterized with automated probing of the fabricated MOS test structures as described below.

Field: represents the breakdown voltage under constant current stressing (CCS) of a large area flat plate gate oxide capacitor with multiple active areas and a LOCOS field edge.

Poly: represents the breakdown voltage of a flat plate gate oxide capacitor with a large perimeter gate edge.

Area represent the breakdown voltage a flat plate gate oxide capacitor with a single field edge.

RESULTS AND DISCUSSION

Ellipsometry: Oxide thickness values measured by ellipsometry for the different cleaning splits showed values within 5% of the targeted oxide thickness. As expected pre-gate cleans which produced a hydrophilic surface by growing a chemical oxide resulted in slightly thicker films than HF-last cleans which removed any surface oxides.

Particle Contamination: All the pre-gate cleans showed a reasonable number of particle adders for this threshold level. However, it is evident that the RCA clean using standard concentrations produced the highest contamination levels. The dilute RCA with dHCl inject to replace the SC2 step showed the best particle performance with less than 10 adders per run while the standard RCA process showed higher particle counts ~25@ 0.12μm. The particle contamination results are summarized in Figure 2.

Metallic Contamination levels were also comparable among splits, with the one exception being the Ref. RCA pre-gate clean showed a higher levels of Al, Zn, and Na. This might be due to using standard/high concentrations of SC1 and SC2. dRCA showed the best metal contamination levels for all metals at detection limit or lower than detection limit levels. For the dRCA, HF-last and HF-last w/HCl, the contamination levels met the ITRS roadmap for the 130nm technology node (11)

Surface Roughness: Surface uniformity is important, since it reduces large gate leakage currents through weak points where the oxide is thinner. Smoothness is also critical to higher carrier mobility. Gong and coworkers have also reported Q_{BD} differences for injection from Si/SiO_2 interface as compared to the $Poly\text{-}Si/SiO_2$ interface based on roughness differences (12). The surface roughness values measured after each of the major clean splits are summarized in Table I. The dRCA clean was the only one which met the ITRS roadmap specification for the 130nm technology node. Figure 3 below shows an AFM image after a dilute RCA pre-gate clean.

Gate Oxide Integrity

Charge to Breakdown Measurements: Ramped voltage was performed on the fabricated test devices to determine the total charge to breakdown value, Q_{BD}, for each of the cleaning splits (13). These results demonstrate a statistically significant improvement in Q_{BD} with the dRCA clean. Additional manual probing was performed using Constant Voltage Stressing (CVS) and Constant Current Stressing (CCS) to characterize the nature of charge trapping occurring. These results correlated well with the ramped voltage data. These results are summarized in Figures 4-6.

Electric Field Breakdown Measurements: The breakdown electric field strength, E_{BD}, was measured on the fabricated test devices using the standard ramped voltage technique to determine the breakdown voltage at a pre-determined current level. This testing was

performed using an automated probe station. The breakdown electric field strength was calculated using the measured oxide thickness to account for variations in final oxide thickness that were noted with the different pre-gate cleans. A higher E_{BD} value indicates a better quality oxide, since a high E_{BD} implies that the film contains a smaller number of charge trapping defects which enhance the internal electric field and result in earlier breakdown.

Results of these measurements for the different test structures are summarized in Figure 7. The E_{BD} averaged ~ 15 MV/cm for all the pre-gate clean splits, which is high for a typical 40Å gate oxide. This is most likely due to the presence of nitrogen in the oxy-nitride stack, which has been shown to reduce charge trapping via stress reduction at the interface. [2]

CONCLUSION

Extensive characterization of the impact of pre-gate cleans on the GOI of nitrided oxides has shown that these dielectrics are relatively insensitive to surface preparation conditions. However, a slight improvement was demonstrated using advanced dilute RCA (dRCA) pre-gate cleaning processes that incorporated combined process/rinse/dry in the same chamber. The dRCA resulted in the lowest particle contamination levels, lowest surface roughness, and best charge to breakdown values. There was no dramatic difference between the dRCA Vs Ref. RCA for the very-thin oxides, however, as the device geometries became smaller and into the high-K materials, the effect of different surface preparation method can be anticipated to become more critical for device reliability. This is due to higher leakage currents and soft Vs hard breakdown mechanisms.

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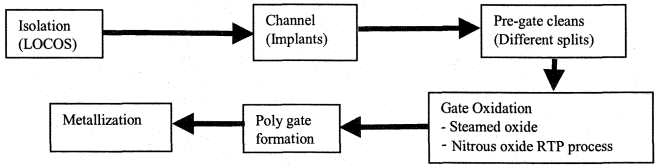


Figure 1: Fabrication Process flow

Table I : Rougness values for the different pre-gate cleans

Pre-gate Clean	*RMS Roughness(Å)*
dRCA	1.08
Conc. RCA	1.43
HF-last	1.63
(HF+HCl)-last	1.68

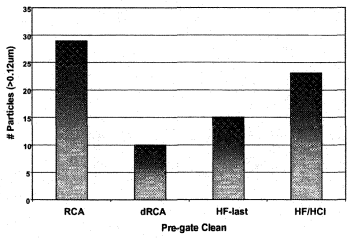
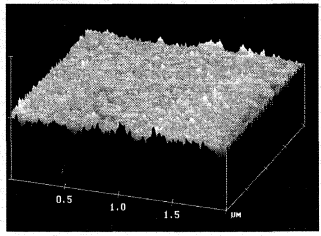


Figure 2: Particle performance for the different pre-gate cleans. dRCA is best



Sample size = 2 X 2 µm, (Rq) = 0.108, Ra = 0.087

Figure 3: AFM Image of wafer surface after a dRCA clean

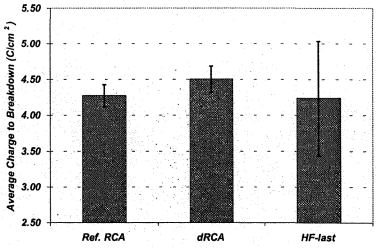


Figure 4: Average charge to breakdown by ramped voltage. dRCA is best

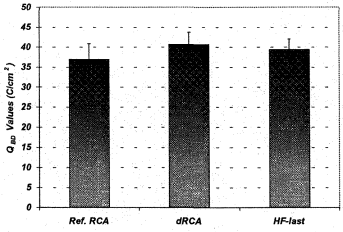


Figure 5: Average charge to breakdown by constant current stressing. dRCA is best

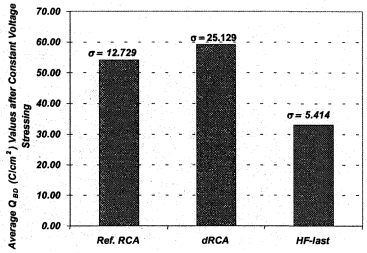


Figure 6: Charge to breakdown for the different cleaning splits after constant voltage stressing. dRCA is best

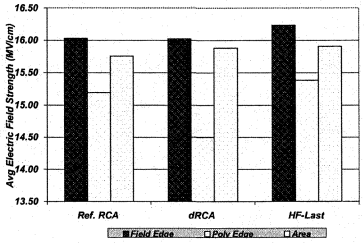


Figure 7: Breakdown electrical field strength MV/cm for the 3 different capacitors

EFFECT OF COMPOSITION AND POST-DEPOSITION ANNEALING ON THE ETCH RATE OF HAFNIUM AND ZIRCONIUM SILICATES IN DILUTE HF

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The etch behavior of hafnium and zirconium silicates in dilute hydrofluoric acid (0.49%) was investigated with respect to film composition and post-deposition annealing. The etch rate of hafnium and zirconium silicate ranges from 23 Å/min to 1.2 Å/min depending on composition and thermal history. In general, the metal silicate etch rate decreases as the silicon dioxide fraction decreases and the thermal budget increases. The low etch rates are attributed to the densification and crystallization of the silicates after anneal and the low etch rate of the metal oxide component of the metal silicates. After over-etching metal silicate films, post-etch surface analysis indicates residual metal remaining on the silicon surface. Selectivities of metal silicate to silicon dioxide of <0.1 were measured, indicating the need for alternative high-k wet etch chemistries with high selectivity to silicon dioxide and silicon.

INTRODUCTION

As the gate dimensions of complementary-metal-oxide-semiconductor (CMOS) devices approach sub-100 nm, the thickness of the silicon oxynitride dielectric pushes the gate leakage farther into direct tunneling.[1] In this regime, tunneling current increases exponentially as the dielectric thickness decreases. Aggressively scaled devices would benefit from an alternate high dielectric constant (high-k) gate material that enables a thicker dielectric to reduce gate leakage for a given equivalent oxide thickness while also maintaining the high mobility of the silicon dioxide/silicon interface. Silicate materials are being investigated as high-k dielectrics to take advantage of the high permittivity of a binary metal oxide combined with the thermal stability and excellent interfacial properties of SiO_2.[2-3] Hafnium and zirconium silicates are particularly interesting materials, since they are expected to be stable on silicon, exhibit bonding similar to SiO_2 and possess reasonably high-k (~15).[2-3] Although high-k dielectrics may offer some advantages over SiO_2, integration of these materials into a standard CMOS flow remains a challenge. For instance, the knock-on of metal into the source/drain regions may demand the removal of the high-k film before ion implantation, and silicidation of the source/drain regions requires its removal. A wet chemistry to etch high-k dielectrics would be advantageous to avoid plasma damage during a dry etch. Therefore, the wet etch behavior of high-k dielectrics needs to be addressed.

The objective of this work was to investigate the etch rate of hafnium and zirconium silicates in dilute hydrofluoric acid (HF), since HF etches silicon slowly and is commonly used in CMOS process flows. The etch rates were determined as a function of film

composition and annealing and are compared to the etch rates of thermal SiO_2 and physical vapor deposited hafnium oxide. The etch rate of hafnium and zirconium silicates are found to decrease with decreasing SiO_2 fraction and increasing thermal budget. The selectivity (high-k to SiO_2 etch rate ratio) of silicates in dilute HF ranges from 4.0 for an as-deposited silicate to <0.1 for a film subjected to a 1000 °C N_2 anneal.

EXPERIMENTAL

Zirconium silicate films (~180 Å) were deposited using chemical vapor deposition (CVD), and hafnium silicate films (~40-180 Å) were deposited using CVD and physical vapor deposition (PVD). PVD hafnium silicate films were deposited at a nominal HfO_2:SiO_2 ratio of 50:50, and CVD hafnium silicate and zirconium silicate films were deposited at nominal metal oxide (MO_2) to SiO_2 ratios of 20:80, 30:70 or 60:40. The films presented here are pseudo-binary alloys, but for simplicity are referred to as either metal silicates or M-O-Si. Hafnium oxide films (~40 Å) were deposited by PVD. Some high-k films underwent a post-deposition rapid thermal anneal (RTA) in 1 atm N_2 at 1000 °C for 30s or 60s. Thermal SiO_2 (1000 Å), as-deposited high-k films and annealed high-k films were etched in dilute (0.49 %) HF using a spray processor. Pre- and post-etch film thickness was measured by ellipsometry using a single-layer model with a fixed refractive index of 2.1. The etch rate is defined as the slope of a least squares fit to the etched film thickness versus time data. Selectivity is defined here as the high-k etch rate divided by the silicon dioxide etch rate.

Table I. Etch rate and selectivity to SiO_2 of hafnium silicate, zirconium silicate and HfO_2 ranked according to decreasing SiO_2 fraction.

Film	Composition (MO_2 : SiO_2)	RTA	Densification	Etch Rate (Å/min)	Selectivity to SiO_2
SiO_2	0:100	-	-	23	-
CVD Zr-O-Si	20:80	1000 °C N_2 30s	N/A	23	1.0
CVD Hf-O-Si	30:70	-	-	91	4.0
CVD Hf-O-Si	30:70	1000 °C N_2 30s	8.6 %	16	0.7
PVD Hf-O-Si	50:50	-	-	85	3.7
PVD Hf-O-Si	50:50	1000 °C N_2 30s	12.9 %	2	0.08
CVD Hf-O-Si	60:40	-	-	88	3.8
CVD Hf-O-Si	60:40	1000 °C N_2 30s	6.5 %	1.2	0.05
CVD Zr-O-Si	60:40	1000 °C N_2 30s	N/A	2.6	0.1
PVD HfO_2	100:0	-	-	33	1.4
PVD HfO_2	100:0	1000 °C N_2 30s	N/A	<0.1	~0.004

RESULTS AND DISCUSSION

In order to investigate the effect of composition and post-deposition RTA on the etch rates of high-k films, as-deposited and annealed PVD and CVD silicates, PVD hafnium oxide and thermal SiO_2 were etched in dilute HF. Table I summarizes the film, post-deposition treatment, film densification post-RTA, etch rate and selectivity data presented in this work. To provide a baseline for comparison of the high-k dielectric etch rates, the etch rate of thermal SiO_2 in dilute HF is presented in Fig. 1. Consistent with literature values, the thermal SiO_2 etch rate is measured at 23 Å/min.[4]

The effect of post-deposition RTA on the etch rate was studied for PVD hafnium silicate and hafnium oxide. Figure 2 demonstrates the dependence of the PVD hafnium silicate etch rate on thermal budget. The measured etch rate of an as-deposited PVD hafnium silicate is 85 Å/min. Figure 2 shows that annealing reduces the etch rate to 2 Å/min. As presented in Table I, subjecting the hafnium silicate to a 1000 °C anneal densifies the film by ~13%. Figures 3 and 4 display high-resolution TEM images of as-deposited and post-RTA PVD hafnium silicate. The two images clearly indicate a structural change upon RTA, since the as-deposited film is amorphous and the post-RTA film exhibits lattice fringes characteristic of its crystallinity. The etch rate dependence on thermal budget of PVD hafnium oxide is presented in Fig. 5. As-deposited hafnium oxide etched at a rate of 33 Å/min, however the etch rate diminished to <0.1 Å/min after a 1000 °C anneal. Post-deposition annealing noticeably increased the etch resistance of both PVD hafnium silicate and hafnium oxide.

In order to test the effects of film composition on high-k etch rates, CVD hafnium silicate and zirconium silicate with MO_2:SiO_2 ratios of 20:80, 30:70 or 60:40 were etched in dilute HF. Figure 6 presents the effect of composition on the CVD hafnium silicate etch rate. The hafnium silicate etch rate was reduced from 16 to 1.2 Å/min when the

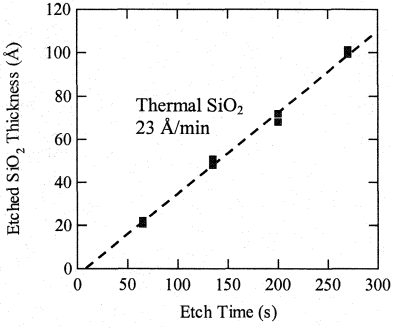

Figure 1. Removal of thermal SiO_2 in dilute HF.

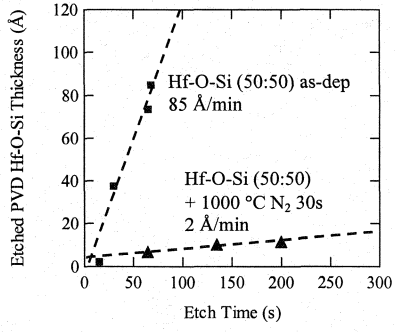

Figure 2. Effect of annealing on the etch rate of PVD hafnium silicate in dilute HF.

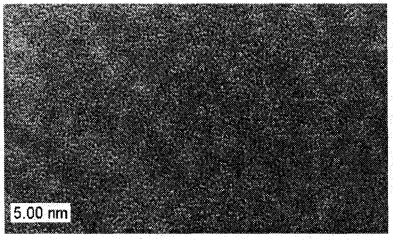

Figure 3. High resolution TEM image of as-deposited PVD Hf-O-Si (50:50).

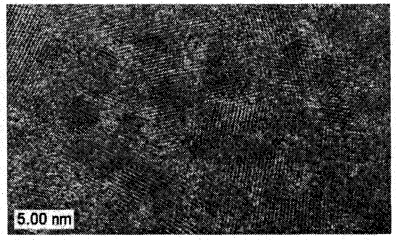

Figure 4. High resolution TEM image of post-RTA (1000 °C, N_2, 60s) PVD Hf-O-Si (50:50).

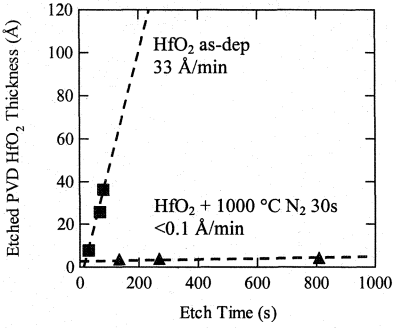

Figure 5. Effect of annealing on the etch rate of PVD hafnium oxide in dilute HF.

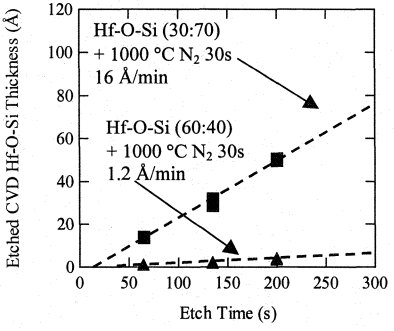

Figure 6. Effect of composition on the etch rate of CVD hafnium silicate in dilute HF.

hafnium silicate composition was changed from silicon-rich (30:70) to metal-rich (60:40). A similar dependence on composition is observed in the CVD zirconium silicate etch rate illustrated in Fig. 7. When the nominal ZrO_2:SiO_2 ratio was increased from 20:80 to 60:40, the zirconium silicate etch rate dropped from 23 to 2.6 Å/min. CVD hafnium silicates exhibit similar as-deposited etch rate, densification behavior and post-RTA etch rate as PVD hafnium silicate. As-deposited CVD hafnium silicates etches at ~90 Å/min for both compositions measured, and post-deposition annealing densified the silicon-rich and hafnium-rich hafnium silicates by 8.6% and 6.5%, respectively (see Table I). Furthermore, post-deposition annealing reduces the etch rates of silicon-rich and hafnium-rich hafnium silicate to 16 Å/min and 1.2 Å/min, respectively. Decreasing silicon dioxide fraction and increasing thermal budget clearly reduces the etch rates of CVD silicates.

In general, high-k etch rate significantly decreases with decreasing silicon dioxide fraction, as displayed in Fig. 8. Figure 8 presents the etch rate of hafnium and zirconium silicate, hafnium oxide and SiO_2 as a function of silicon dioxide fraction.

The etch rate decreased by over two orders of magnitude when the SiO_2 fraction was changed from 100% to 0%, and the etch rate closely followed an exponential dependence on the SiO_2 fraction.

As-deposited and annealed (1000 °C, N_2, 60s) PVD hafnium silicate films (~40 Å) were etched to test the ability of dilute HF to completely clear silicate from a silicon wafer. The films were etched for a fixed time that represents an over-etch of 10X and 4X for the as-deposited and annealed films, respectively. Bulk film removal was confirmed by ellipsometry, and the post-etch wafers measured <5 Å optically. The post-etch wafers

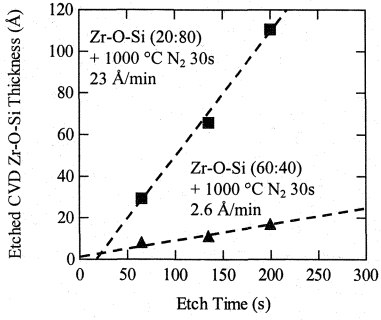

Figure 7. Effect of composition on the etch rate of CVD zirconium silicate in dilute HF.

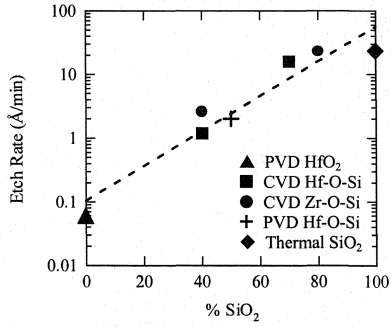

Figure 8. Effect of the silicon fraction on the etch rate of hafnium and zirconium silicate, HfO_2 and SiO_2 in dilute HF.

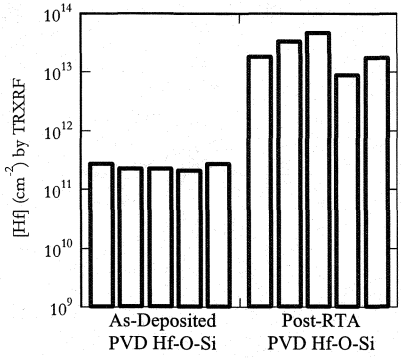

Figure 9. TRXRF hafnium concentration on the silicon surface of etched as-deposited and post-RTA (1000 °C, N_2, 60s) PVD hafnium silicate wafers.

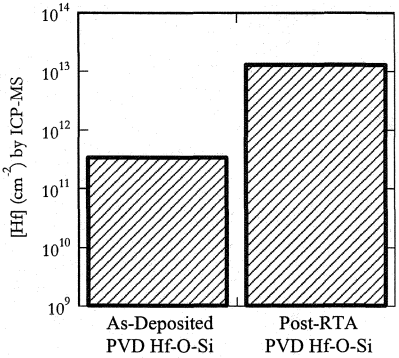

Figure 10. ICP-MS hafnium concentration on the silicon surface of etched as-deposited and post-RTA (1000 °C, N_2, 60s) PVD hafnium silicate wafers.

were analyzed for hafnium contamination by total reflection x-ray fluorescence (TRXRF) and inductively coupled plasma mass spectrometry (ICP-MS). Figure 9 displays the TRXRF results analyzed at five sites per wafer across two wafers. TRXRF showed hafnium contamination at $3x10^{11}$ and $3x10^{13}$ cm^{-2} for the etched as-deposited and annealed hafnium silicate wafers, respectively. ICP-MS results for post-etch wafers are presented in Fig. 10. ICP-MS showed $4x10^{11}$ and $1x10^{13}$ cm^{-2} of hafnium contamination for the etched as-deposited and annealed hafnium silicate wafers, respectively. Since a monolayer on Si(100) represents a concentration of ~10^{14} cm^{-2}, sub-monolayer coverage of hafnium exists on the surface of the post-etch wafers, however the concentrations are still high enough to possibly inhibit silicide formation or result in knock-on during implantation.

The results presented above illustrate that the etch rate of silicates in dilute HF can be much greater or much less than that of thermal SiO_2 depending on the composition and the thermal history of the film, as indicated by the selectivity data compiled in Table I. For example, the selectivity (3.7) of as-deposited PVD hafnium silicate to SiO_2 dropped sharply to 0.08 after a 1000 °C anneal. The densification [5, 6] and crystallization upon high temperature annealing of the silicate explains the resultant decrease in the etch rate. The selectivity of annealed CVD hafnium and zirconium silicate decreased by an order of magnitude from ~1 to ~0.1 when the composition was changed from silicon-rich to metal-rich. The low etch rate of metal-rich silicate films can be attributed to the low etch rate of the metal oxide component, as demonstrated here for hafnium oxide. Furthermore, the etch rate of silicates can be similar to SiO_2 when the SiO_2 fraction is high, as in the case of annealed 30:70 CVD hafnium silicate and 20:80 CVD zirconium silicate where the selectivities to SiO_2 are 0.7 and 1, respectively. Although dilute HF achieves the bulk removal of metal silicates, aggressive over-etching is insufficient at completely removing the residual metal contamination from the wafer surface.

The etch rate of PVD hafnium oxide exhibits a stronger dependence on thermal budget compared to PVD hafnium silicate. The selectivity of as-deposited PVD hafnium oxide changed from 1.4 to ~0.004 after a 1000 °C anneal. The 1000 °C anneal crystallized the hafnium oxide (TEM not shown), which in part accounts for the drastic drop in the etch rate. Comparing the etch rates of annealed PVD hafnium silicate and hafnium oxide (2 and <0.1 Å/min, respectively) reveals the chemical inertness of HfO_2 in dilute HF and illustrates the difficulty of integrating metal oxides into a standard CMOS process flow.

Low selectivity of high-k dielectrics to SiO_2 can be problematic when attempting to clear high-k films from silicon and SiO_2 regions simultaneously. Without high selectivity to both SiO_2 and silicon, over-etching high-k dielectrics under these conditions could lead to excessive removal of SiO_2 from the isolation or silicon from the substrate regions of a device. Integration of high-k dielectrics may require new etch processes with high selectivity to SiO_2 and silicon.

CONCLUSIONS

This work reports on the effects of composition and post-deposition RTA on the etch rates of hafnium and zirconium silicates in dilute HF. In general, the etch rate decreases as the silicon content decreases and the thermal budget increases. Also, the degree of densification and crystallization play important roles in determining the etch behavior of high-k films. If a silicate has a high SiO_2 fraction and/or a low thermal budget, then HF may be an appropriate silicate etch. However, if a silicate has a low SiO_2 fraction and/or a high thermal budget, then HF may not be a suitable etch, since a significant amount of the isolation may be removed during silicate over-etch. These results indicate that the composition and thermal history of hafnium and zirconium silicates must be taken into account when choosing a wet etch process, and that alternate etch chemistries may need to be developed for high-k dielectrics.

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AUTHOR INDEX

SUBJECT INDEX